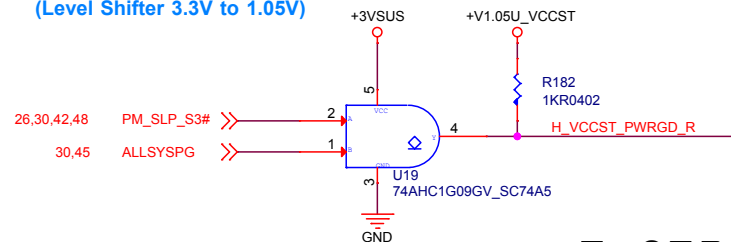


## VCCST\_PWRGD (Level Shifter 3.3V to 1.05V)



I7-8750H

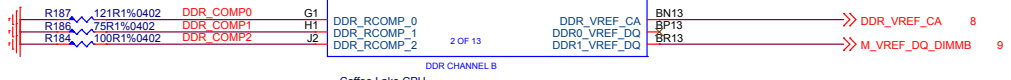
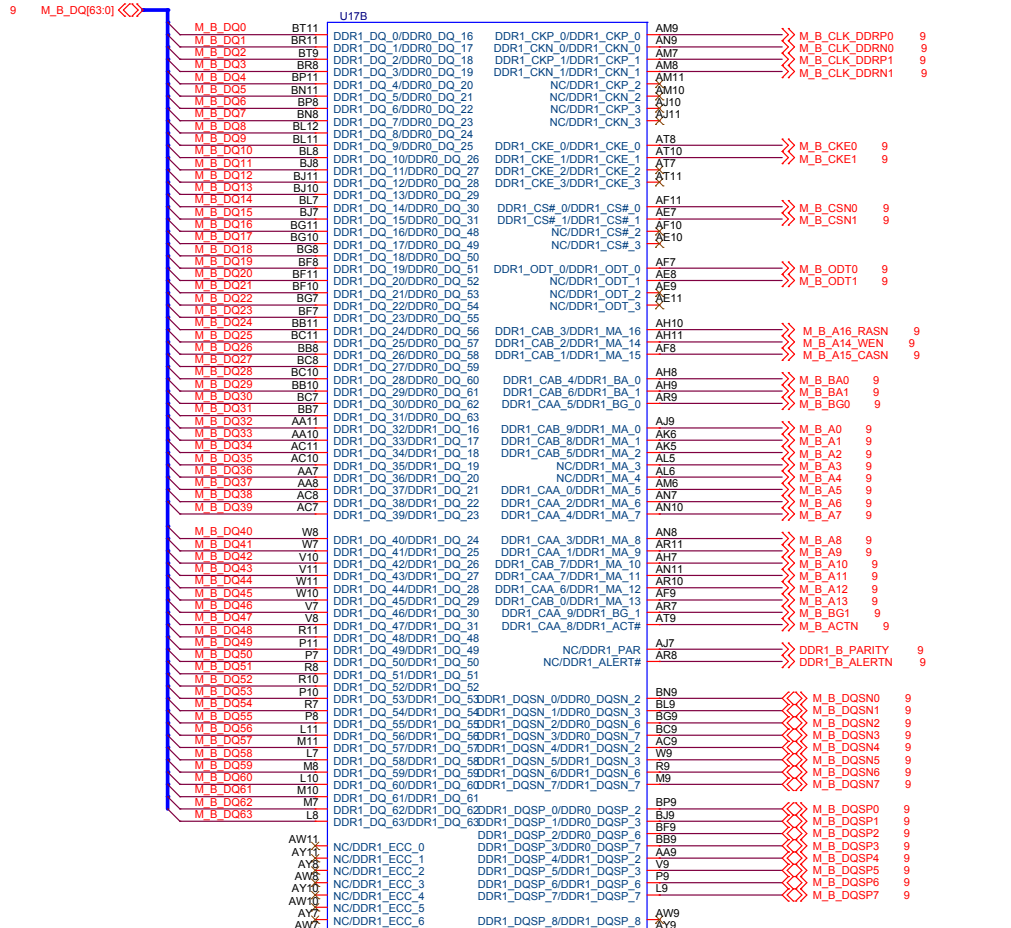
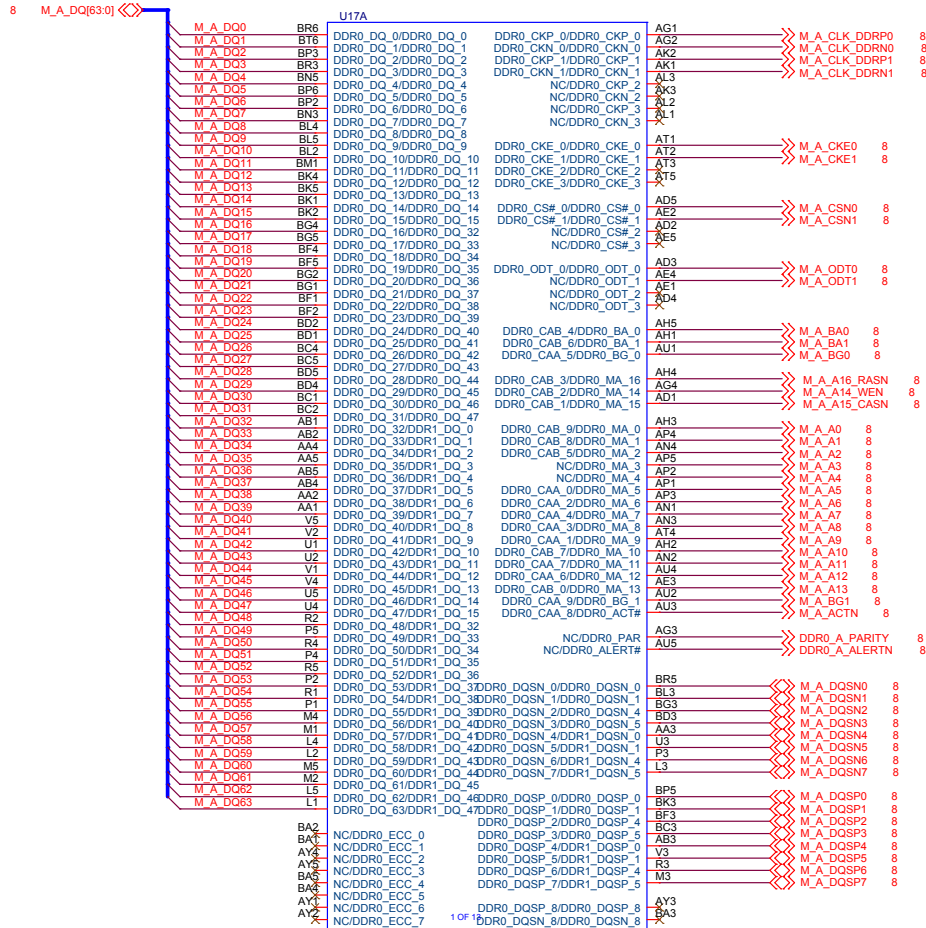
I7\_8750  
A0D-8750H05-I06  
X\_I7-8750

I5-8300H

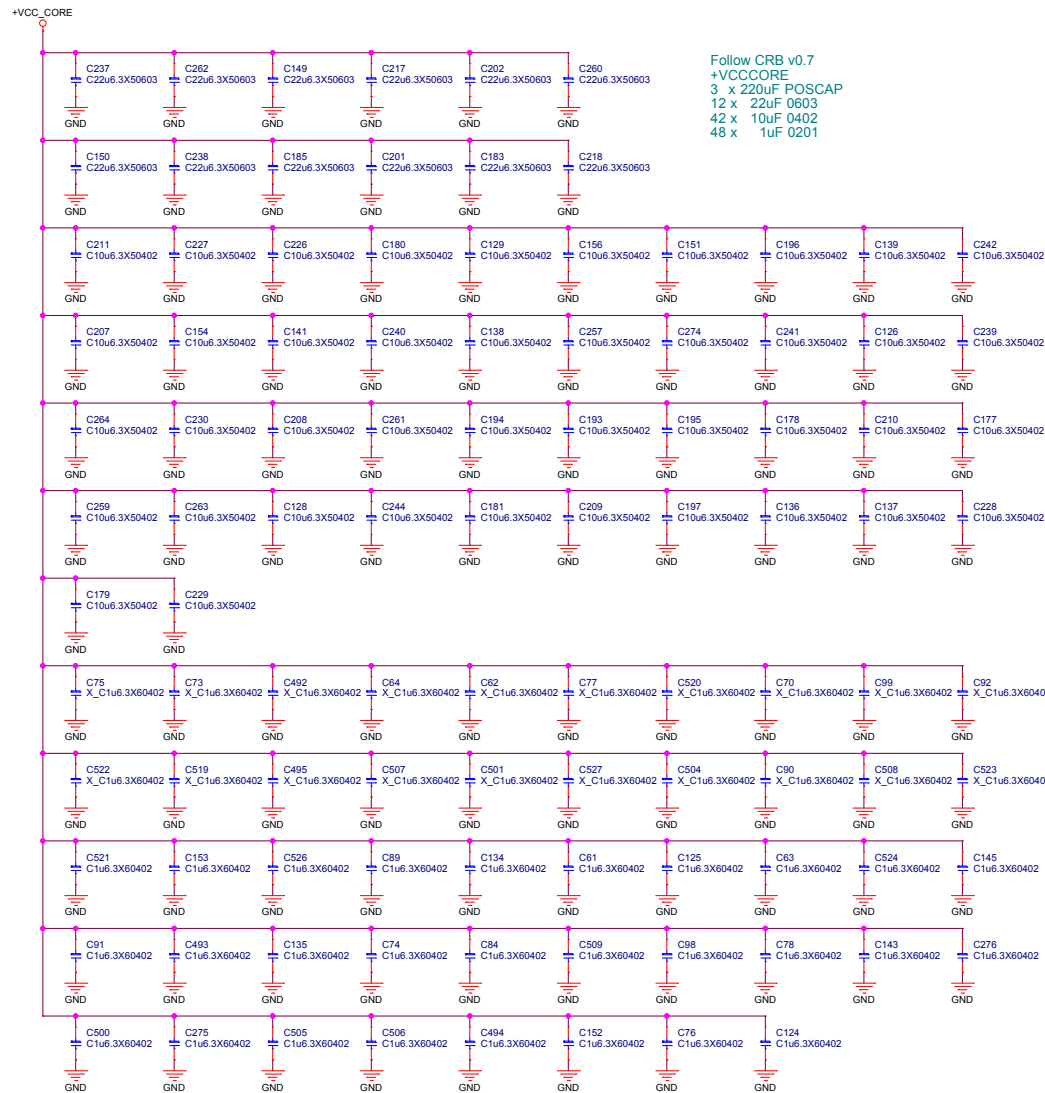
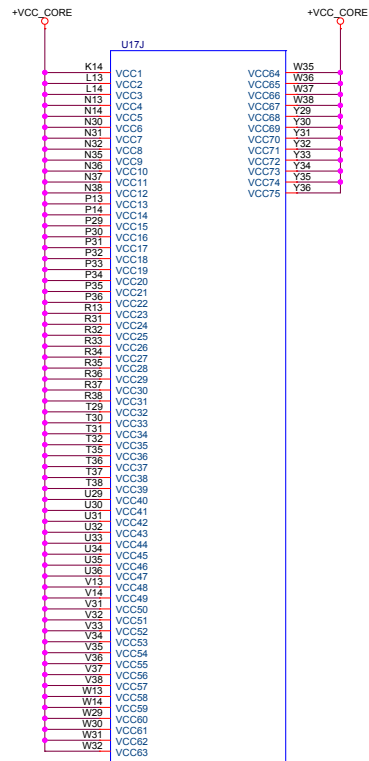
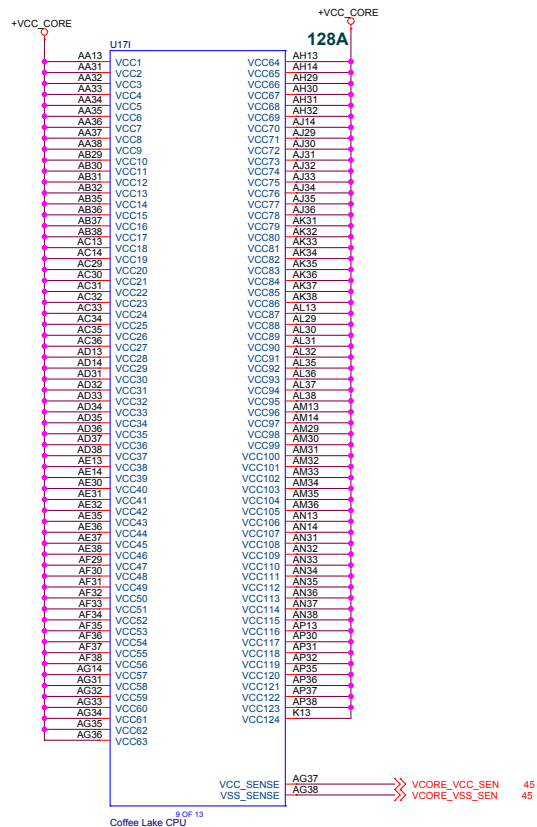
I5\_8300  
A0C-8300H05-I06  
X\_I5-8300

# DDR Channel A

# DDR Channel B

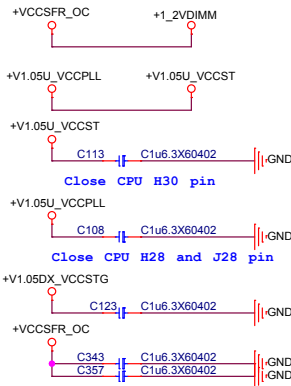
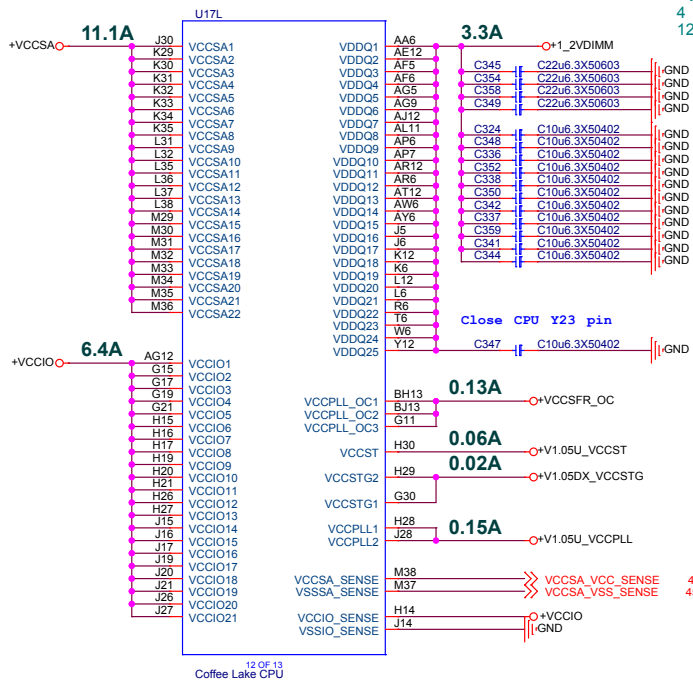




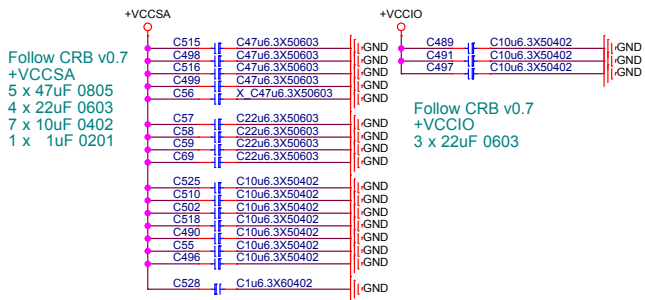
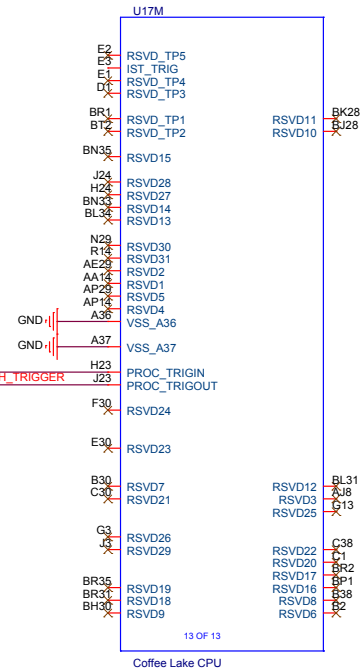


Follow CRB v0.7  
+VCCCORE  
3 x 220uF POSCAP  
12 x 22uF 0603  
42 x 10uF 0402  
48 x 1uF 0201

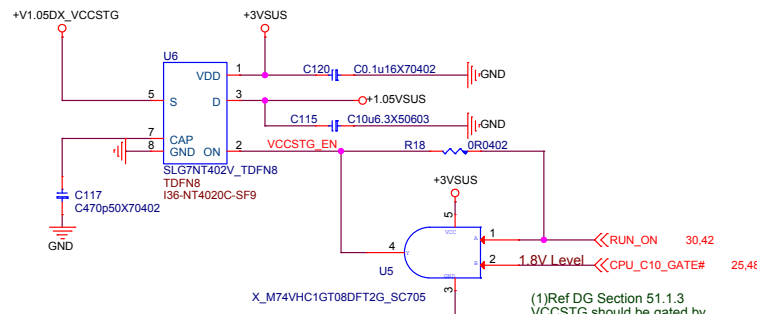
Follow CRB v0.7  
+VCCDU (+1.2V DIMM)  
4 x 22uF 0603  
12 x 10uF 0402



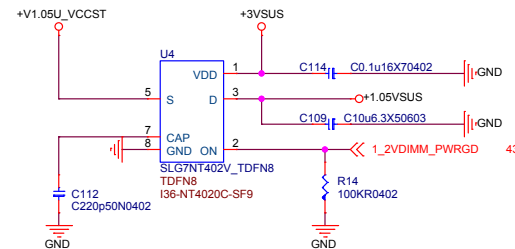
24 PCH\_2\_CPU\_TRIGGER\_R  
24 CPU\_2\_PCH\_TRIGGER\_R



## +V1.05DX\_VCCSTG



## +V1.05U\_VCCST

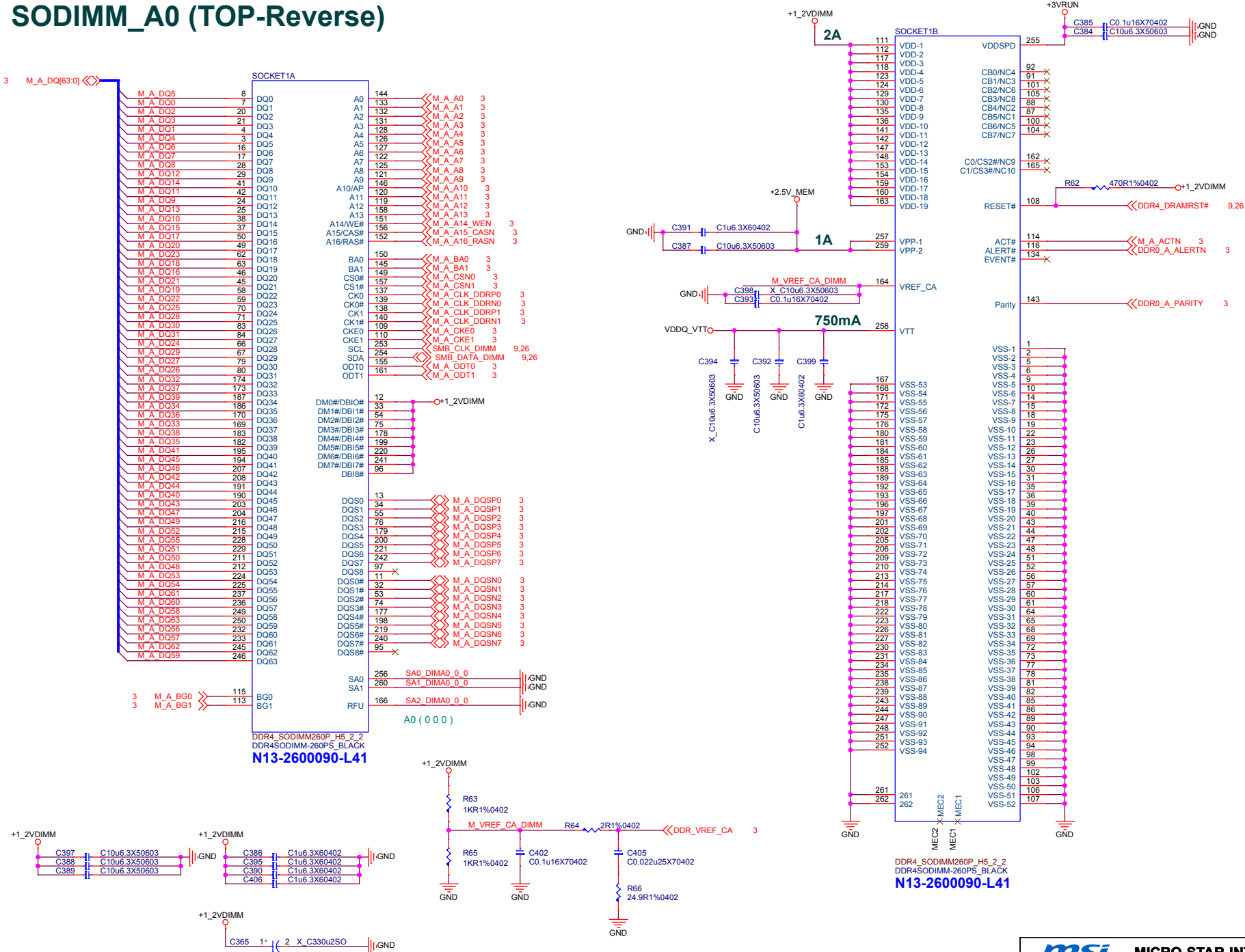


(1)Ref DG Section 51.1.3  
VCCSTG should be gated by  
(SLP\_S3#) AND (CPU\_C10\_GATE#)  
(2)Power Sequence spec iCPU26  
CPU\_C10\_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us





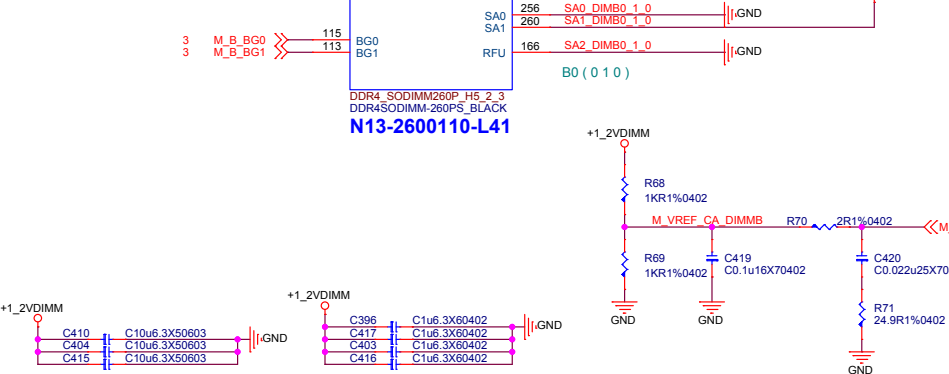
SODIMM\_A0 (TOP-Reverse)






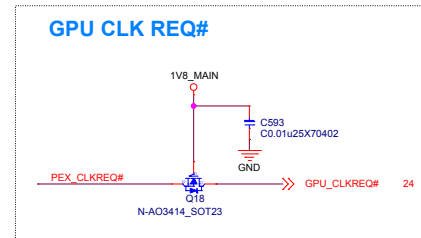
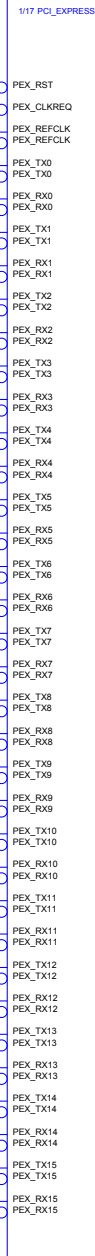
**M\_B\_DQ[63:0] Pinout**

Pin	Signal	Direction	Signal	Direction
1	M_B_DQ0	8	DQ0	
2	M_B_DQ5	7	DQ1	
3	M_B_DQ7	20	DQ2	
4	M_B_DQ3	21	DQ3	
5	M_B_DQ4	4	DQ4	
6	M_B_DQ2	3	DQ5	
7	M_B_DQ1	16	DQ6	
8	M_B_DQ6	17	DQ7	
9	M_B_DQ9	28	DQ8	
10	M_B_DQ14	29	DQ9	
11	M_B_DQ13	41	DQ10	
12	M_B_DQ15	42	DQ11	
13	M_B_DQ8	24	DQ12	
14	M_B_DQ10	25	DQ13	
15	M_B_DQ11	38	DQ14	
16	M_B_DQ12	37	DQ15	
17	M_B_DQ16	50	DQ16	
18	M_B_DQ18	49	DQ17	
19	M_B_DQ21	62	DQ18	
20	M_B_DQ19	63	DQ19	
21	M_B_DQ17	46	DQ20	
22	M_B_DQ22	45	DQ21	
23	M_B_DQ23	58	DQ22	
24	M_B_DQ20	59	DQ23	
25	M_B_DQ25	70	DQ24	
26	M_B_DQ31	71	DQ25	
27	M_B_DQ24	83	DQ26	
28	M_B_DQ28	84	DQ27	
29	M_B_DQ26	86	DQ28	
30	M_B_DQ27	67	DQ29	
31	M_B_DQ30	79	DQ30	
32	M_B_DQ26	80	DQ31	
33	M_B_DQ39	174	DQ32	
34	M_B_DQ35	173	DQ33	
35	M_B_DQ32	187	DQ34	
36	M_B_DQ37	186	DQ35	
37	M_B_DQ34	170	DQ36	
38	M_B_DQ38	169	DQ37	
39	M_B_DQ33	183	DQ38	
40	M_B_DQ36	182	DQ39	
41	M_B_DQ41	195	DQ40	
42	M_B_DQ45	194	DQ41	
43	M_B_DQ46	207	DQ42	
44	M_B_DQ43	208	DQ43	
45	M_B_DQ40	191	DQ44	
46	M_B_DQ44	190	DQ45	
47	M_B_DQ42	203	DQ46	
48	M_B_DQ47	204	DQ47	
49	M_B_DQ55	216	DQ48	
50	M_B_DQ48	215	DQ49	
51	M_B_DQ49	228	DQ50	
52	M_B_DQ51	229	DQ51	
53	M_B_DQ52	211	DQ52	
54	M_B_DQ54	212	DQ53	
55	M_B_DQ53	224	DQ54	
56	M_B_DQ50	225	DQ55	
57	M_B_DQ51	237	DQ56	
58	M_B_DQ62	236	DQ57	
59	M_B_DQ60	249	DQ58	
60	M_B_DQ58	250	DQ59	
61	M_B_DQ59	232	DQ60	
62	M_B_DQ57	233	DQ61	
63	M_B_DQ56	245	DQ62	
64	M_B_DQ63	246	DQ63	
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		MICRO-STAR INT'L CO.,LTD.	
Title			
DDR4 SODIMM B0			
Size	Document Number	Rev	
Custom	MS-16R1	1.0	
Date:	Wednesday, April 11, 2018	Sheet	9 of 57

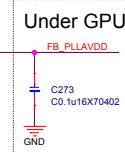
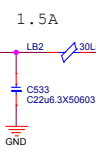
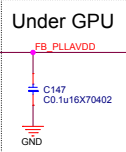
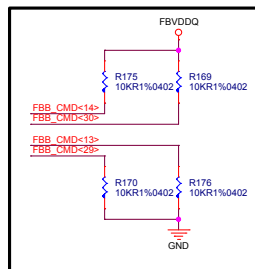
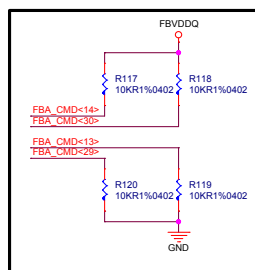
**G1A**  
INS155376830  
COMMON



## GPU Frame Buffer Partition A/B

GDD5 Command Mapping GB4C-128

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3 BA3
CMD2	CMD18	A2 BA0
CMD3	CMD19	A4 BA2
CMD4	CMD20	A5 BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7 A8
CMD7	CMD23	A6 A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12 RFU
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



msi MICRO-STAR INT'L CO.,LTD.

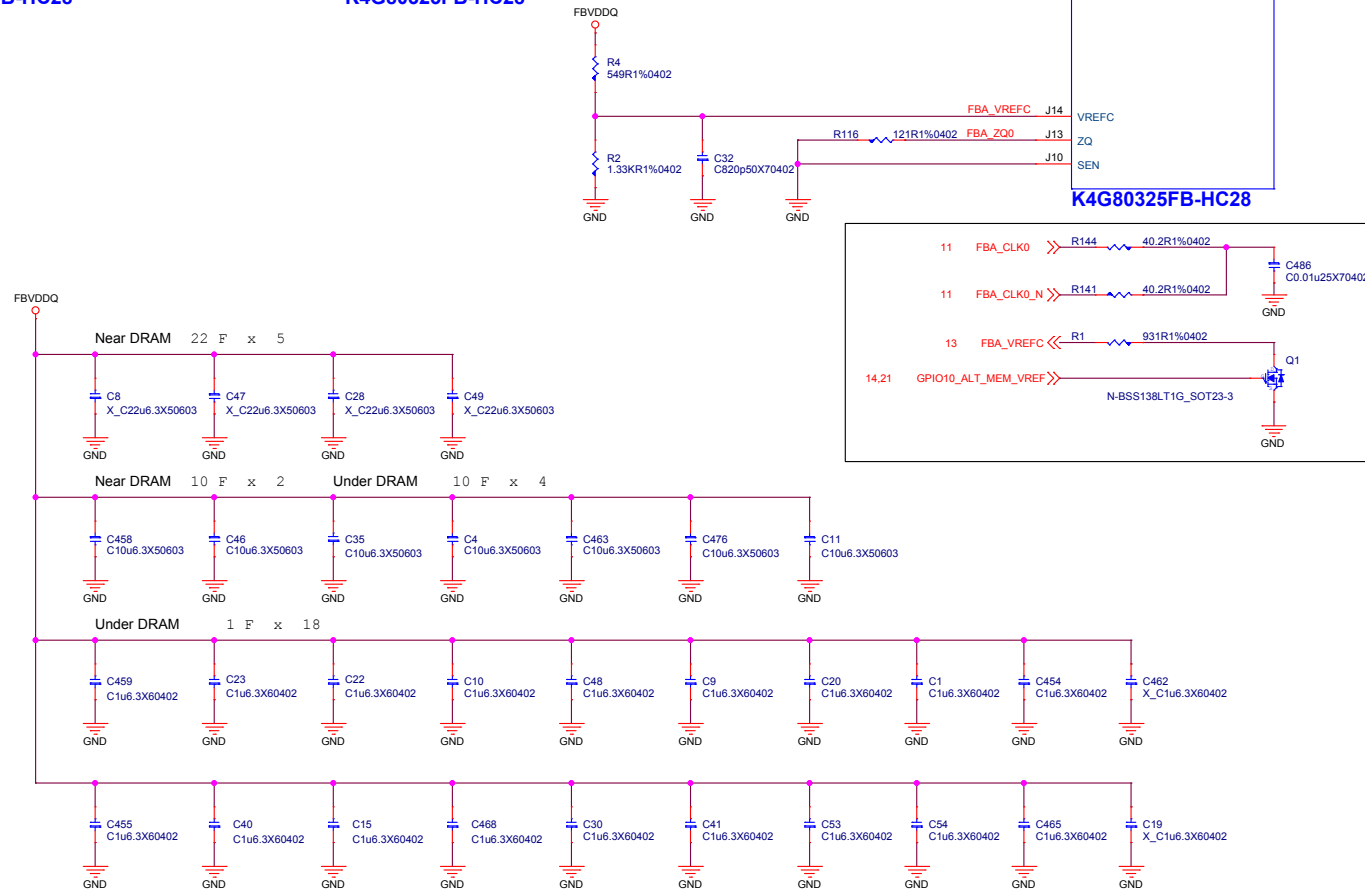
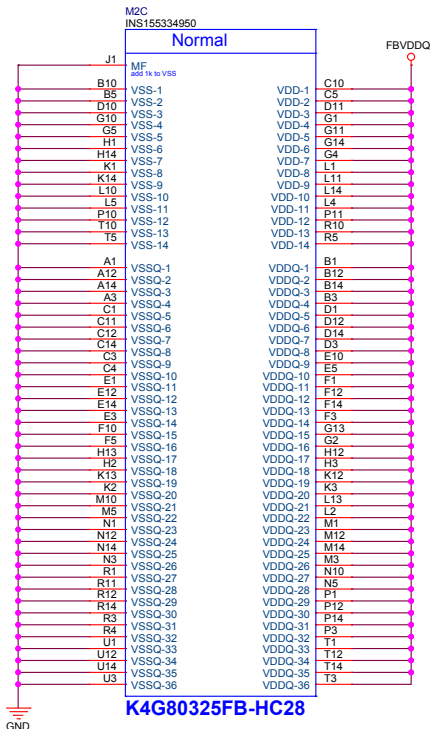
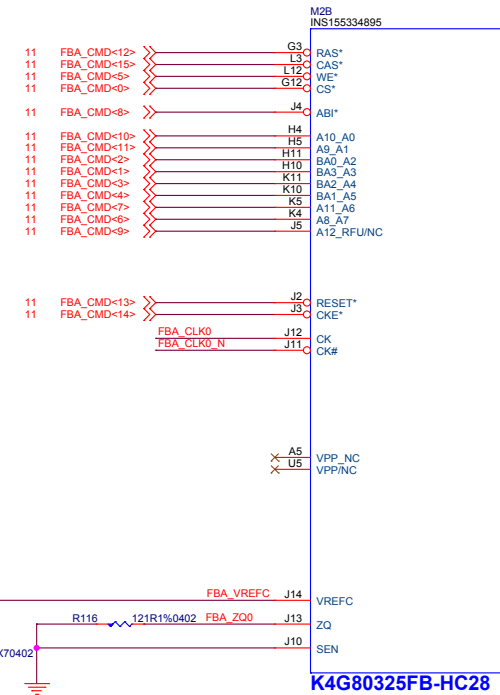
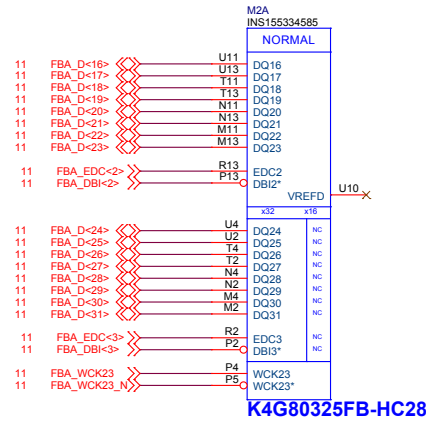
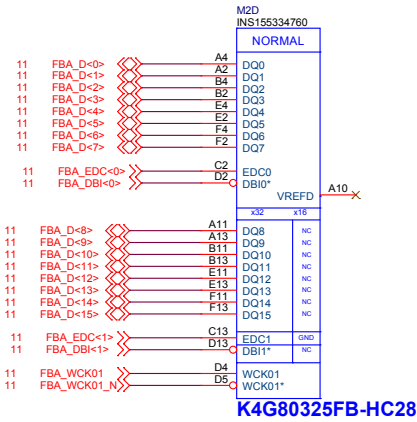
File DGPU MEM IF A/B

Size Customer Document Number MS-16R1

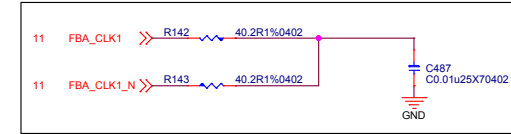
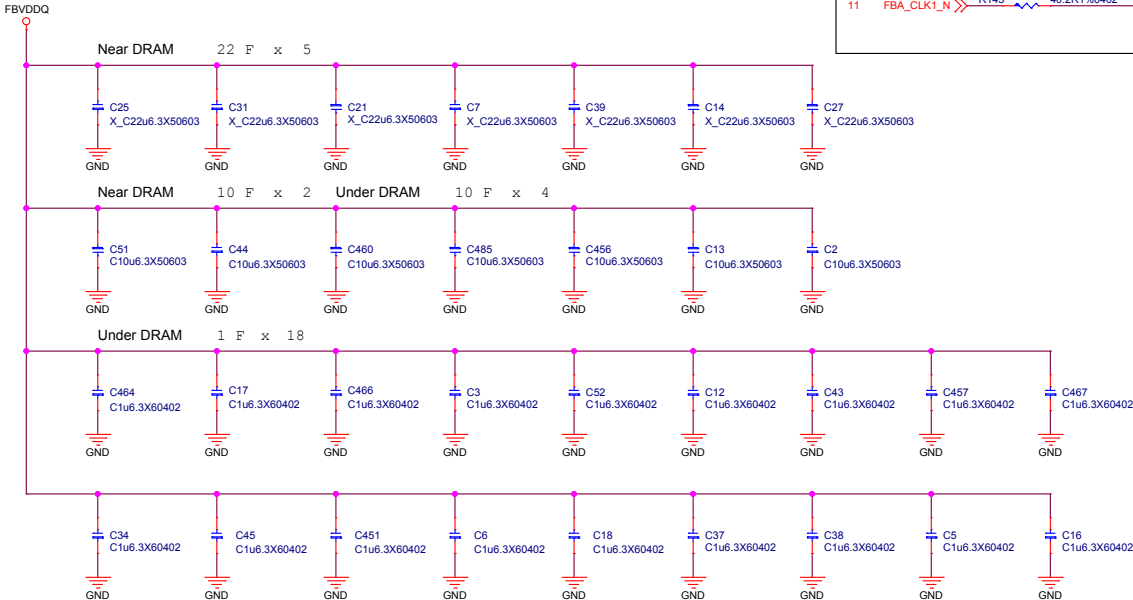
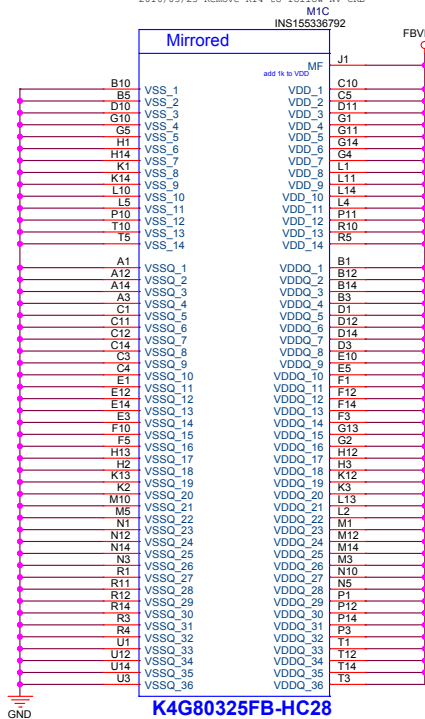
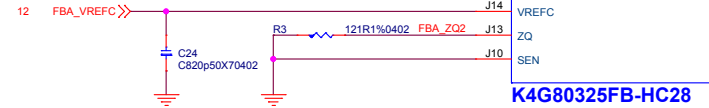
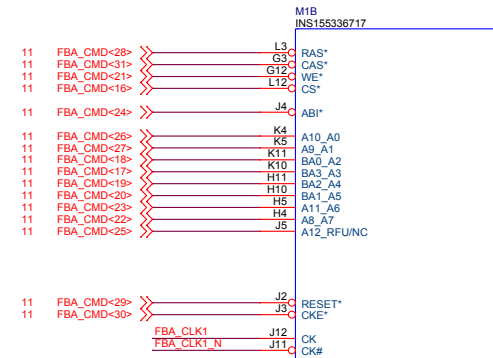
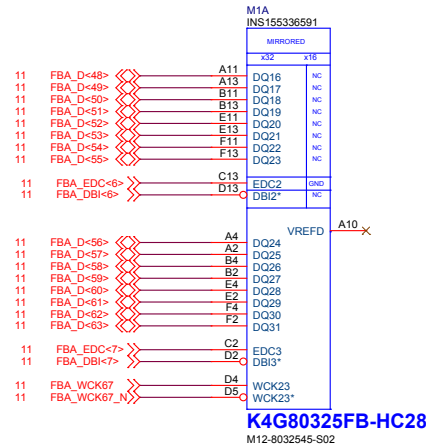
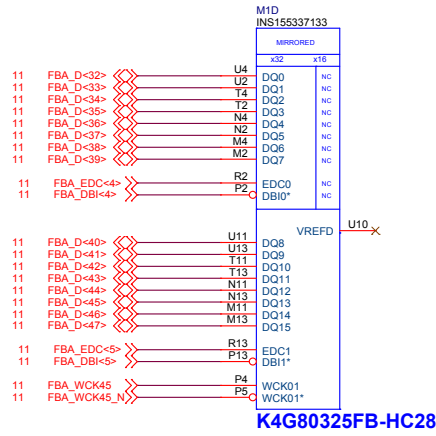
Date: Monday, April 16, 2018 Sheet 11 of 57

Rev 1.0

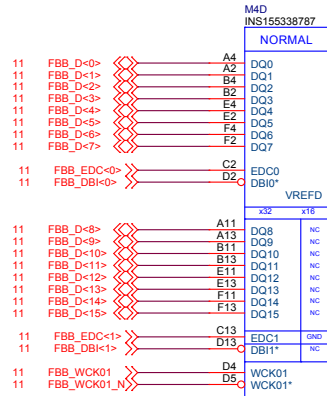
# DGPU\_GDDR5 FrameBuffer A0



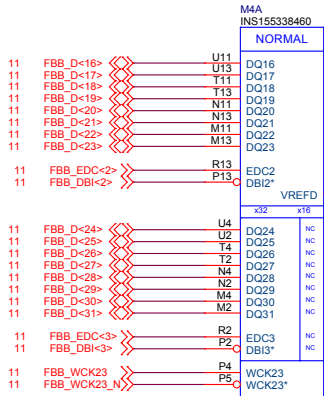
# DGPU\_GDDR5 FrameBuffer A1



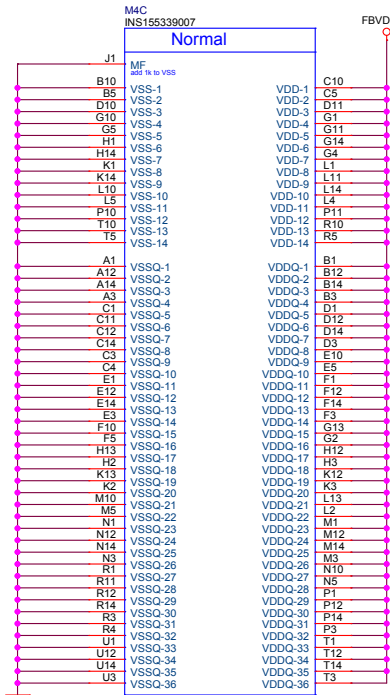
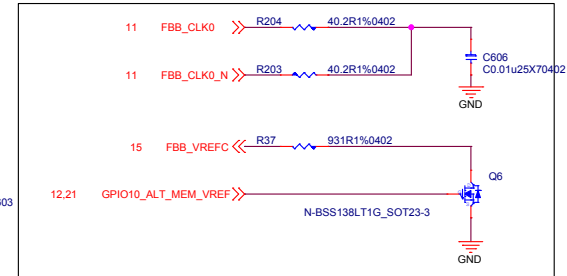
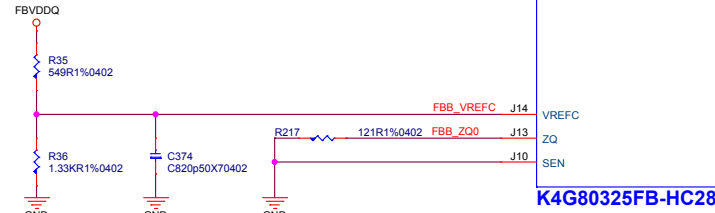
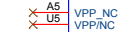
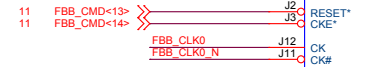
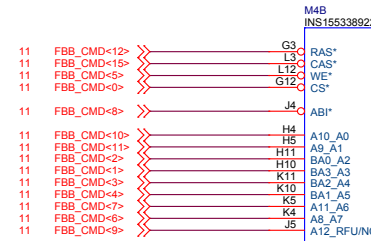
# DGPU\_GDDR5 FrameBuffer B0



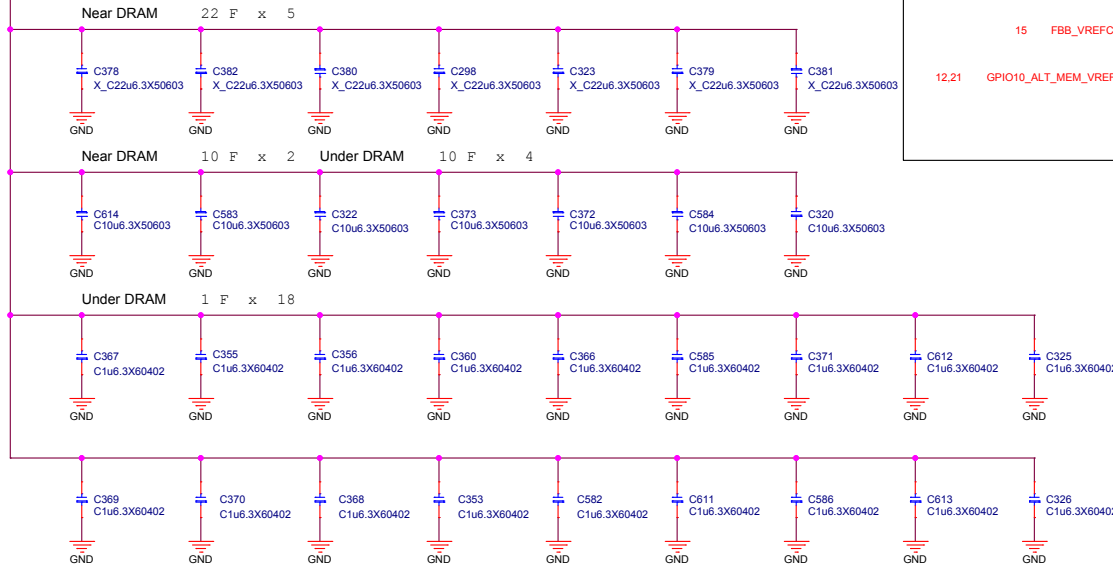
K4G80325FB-HC28



K4G80325FB-HC28

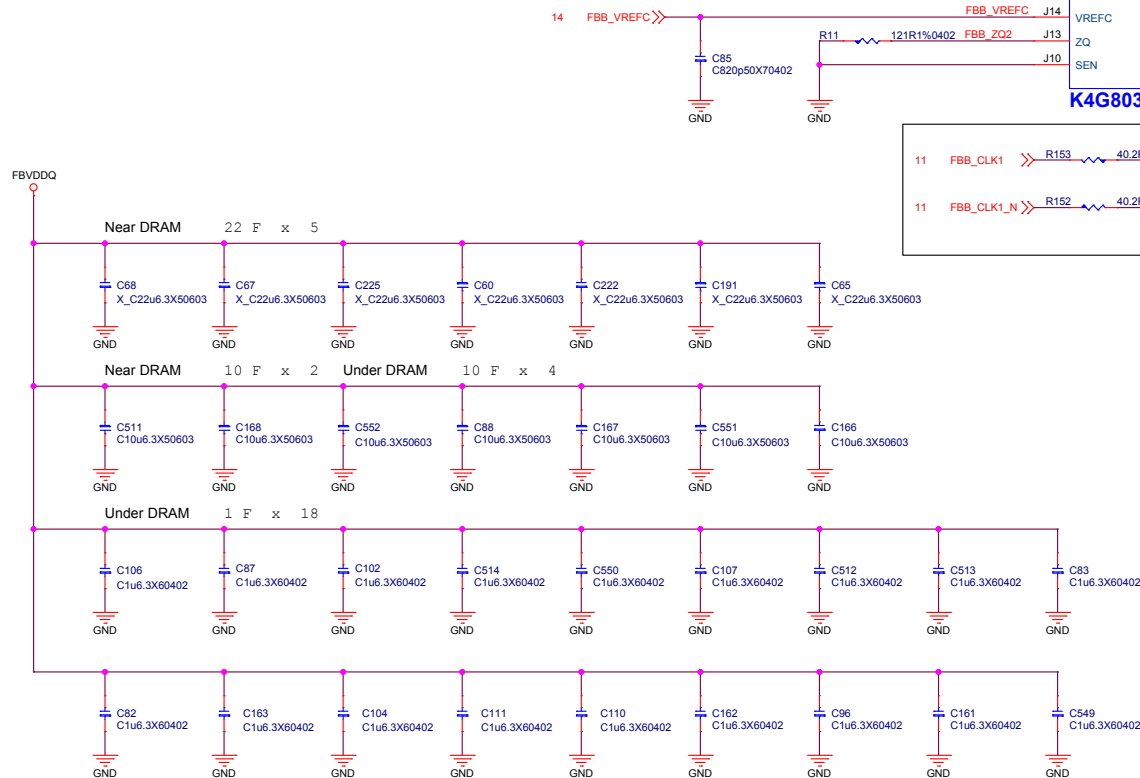
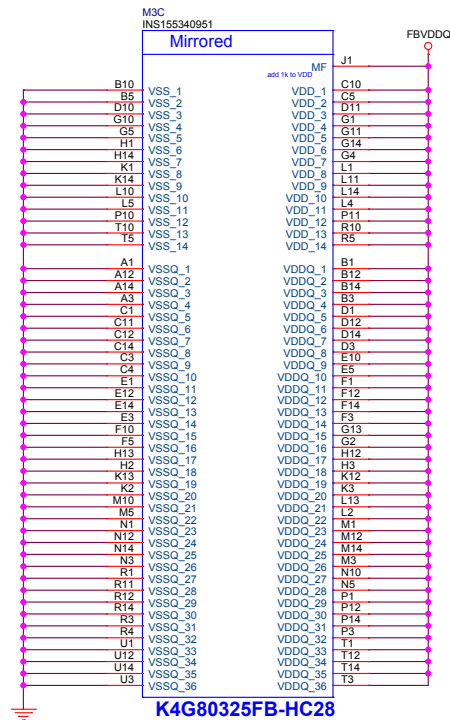
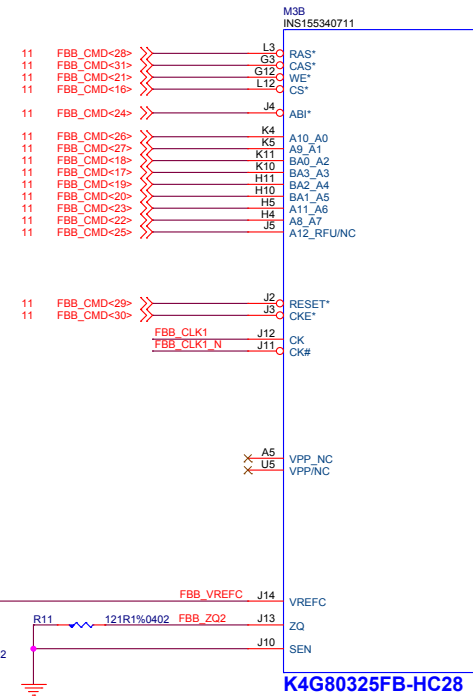
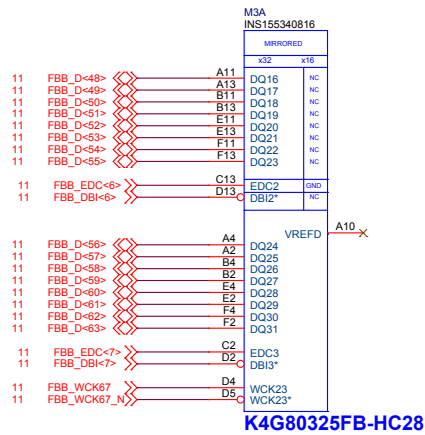
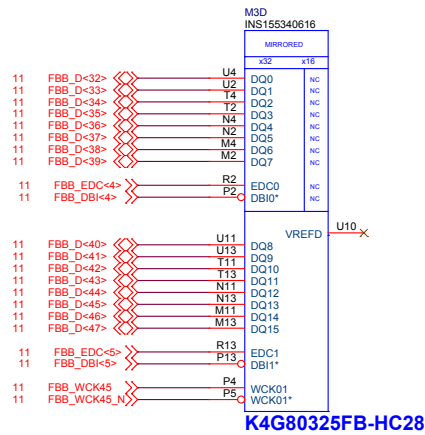


K4G80325FB-HC28

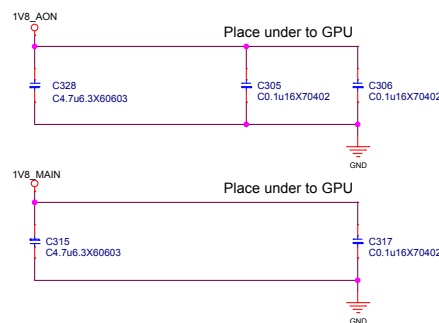
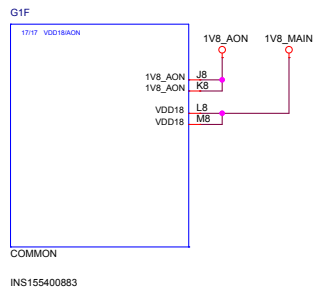
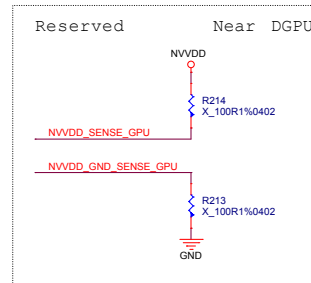
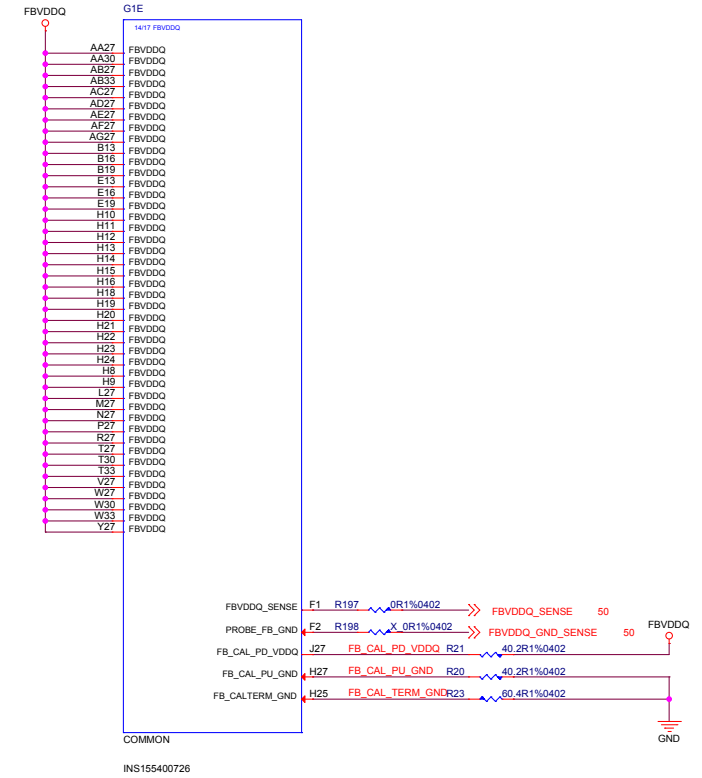
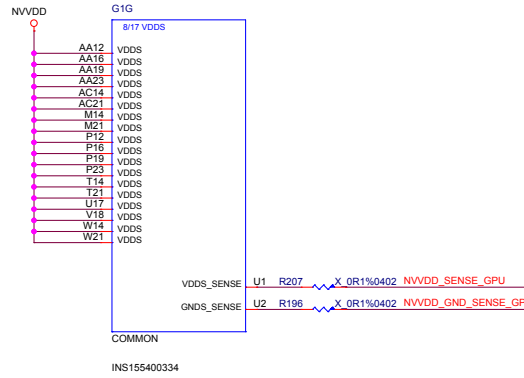
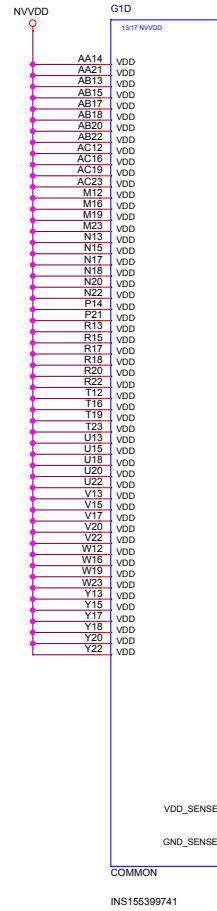
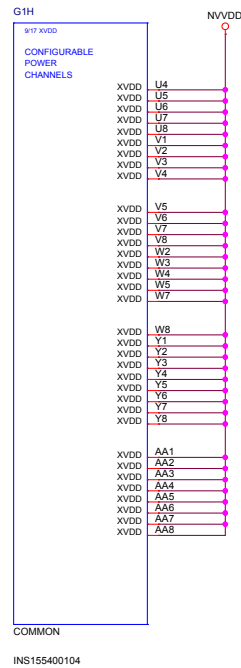




# DGPU\_GDDR5 FrameBuffer B1



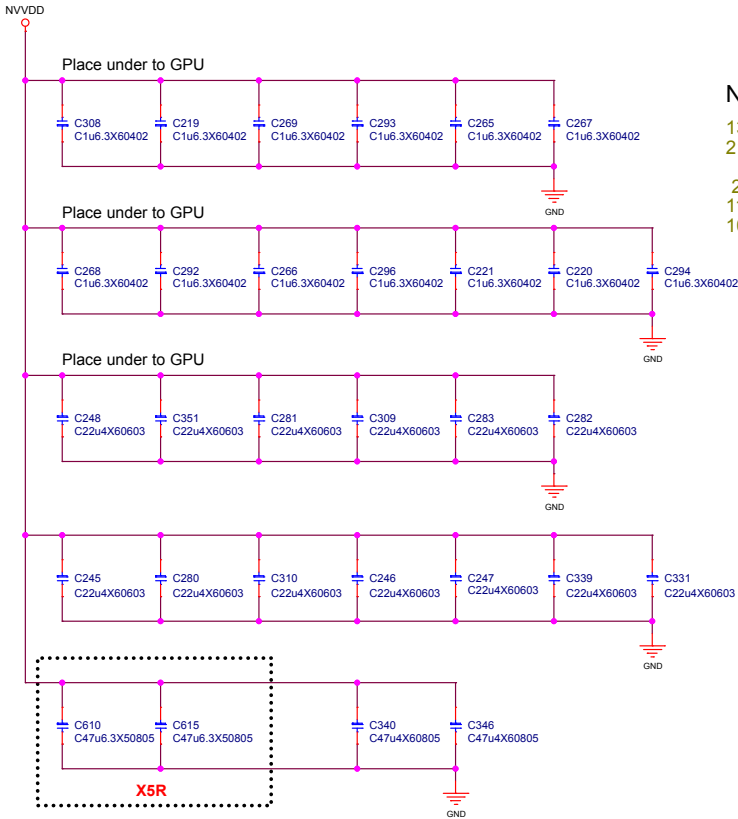
# GPU NVVDD, FBVDDQ



DGPU GND



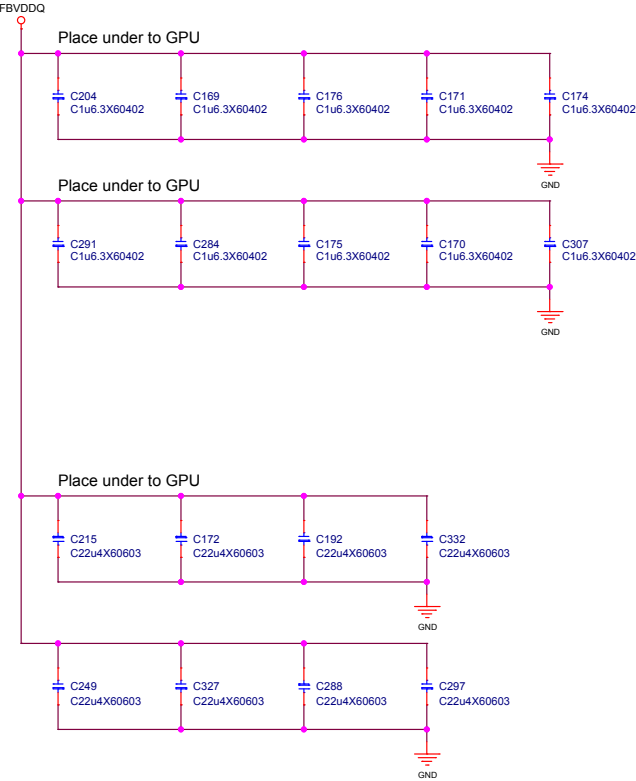
GPU DECOUPLING



NVVDD+NVDDS

13 x 1uF(Under GPU)  
21 x 10uF(Under GPU)

2 x 4.7uF(Near GPU)  
11 x 10uF(Near GPU)  
10 x 22uF(Near GPU)

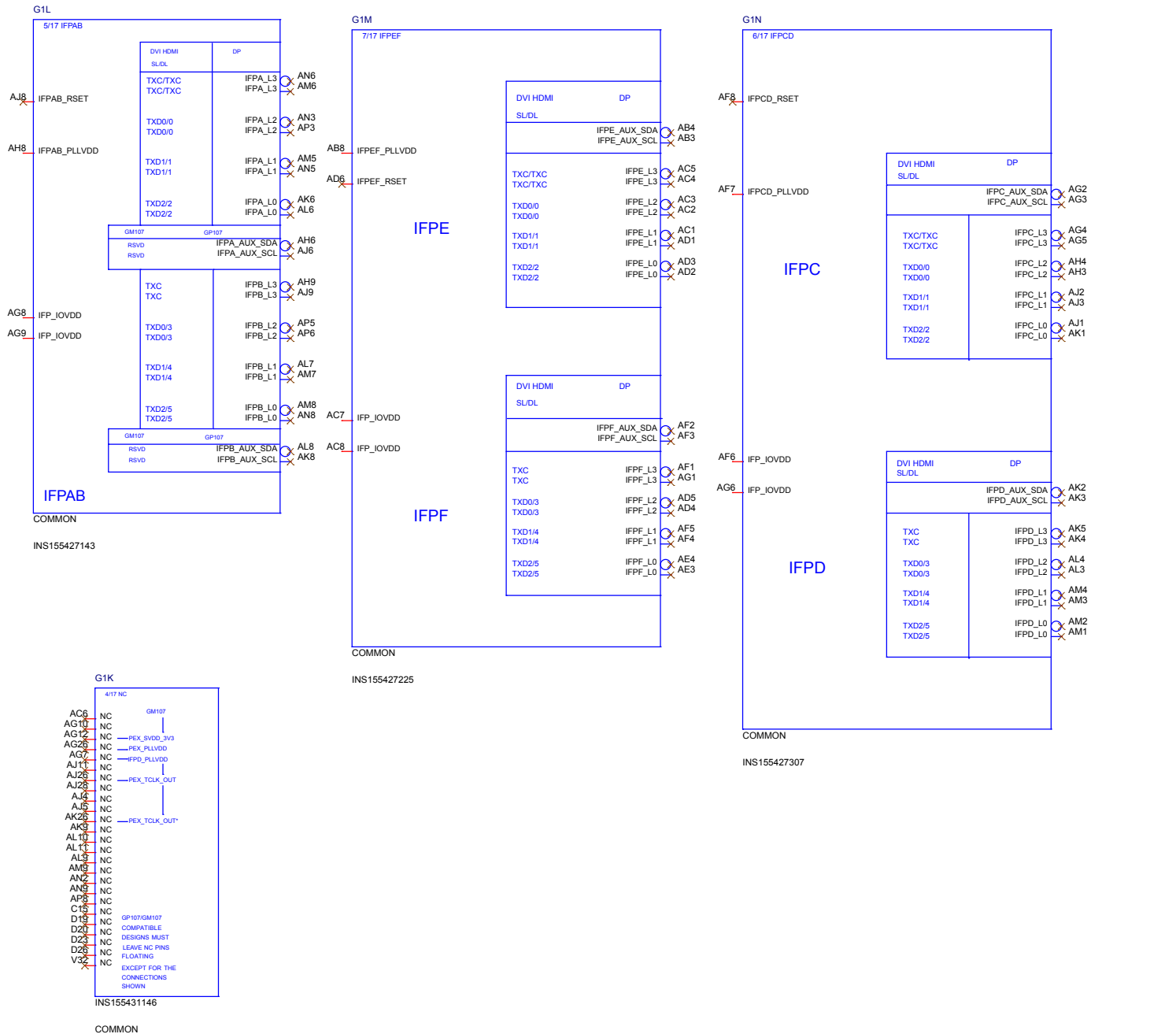


FBVDDQ

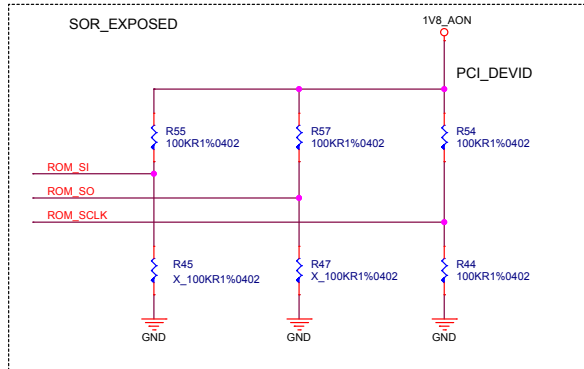
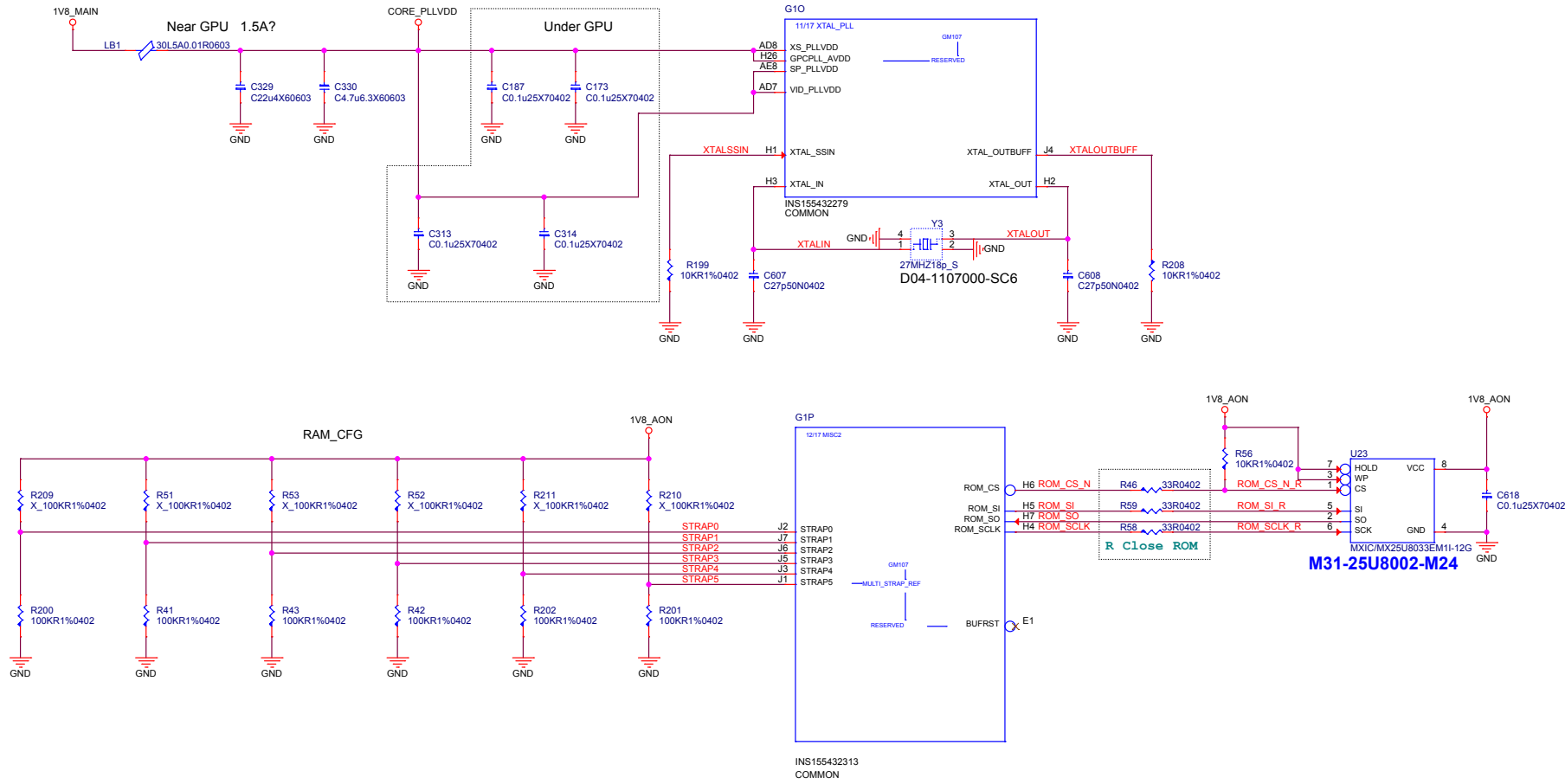
12 x 1uF(Under GPU)  
4 x 10uF(Under GPU)

2 x 10uF(Near GPU)  
5 x 22uF(Near GPU)

# DACA,Display IF



# ROM, MULTI-LEVEL STRAPS



STRAP 5	STRAP 4	STRAP 3	
L	L	L	Optimus
L	L	H	Discrete
H	L	H	Discrete with Gsync

STRAP 2	STRAP 1	STRAP 0		
L	L	L	0x0	Samsung K4G80325FB-HC25
L	L	L	0x0	Samsung K4G80325FB-HC28
L	L	H	0x1	Microm MT51J2256M32HF-80:A
L	H	L	0x2	Hynix H5GC8H24MJR-R4C
H	H	L	0x6	Hynix H5GQ4H24AJR-R4C
H	H	H	0x7	Samsung K4G41325FE-HC25

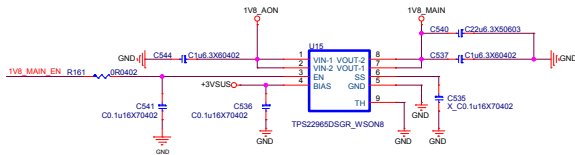
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE



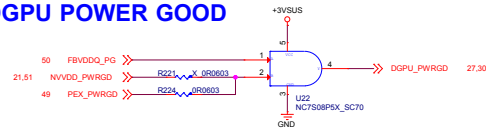
---



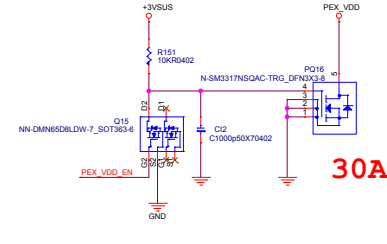
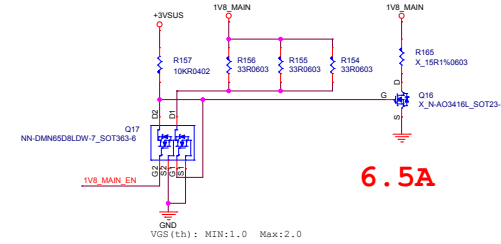
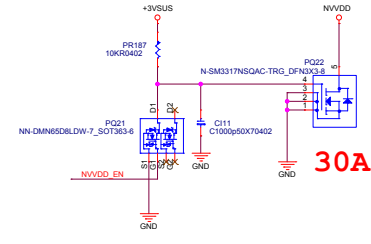
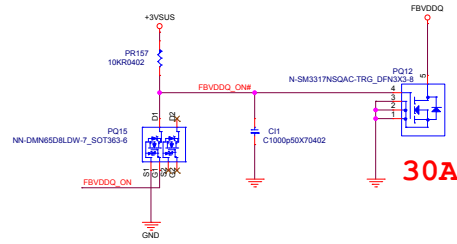
## 1V8\_MAIN



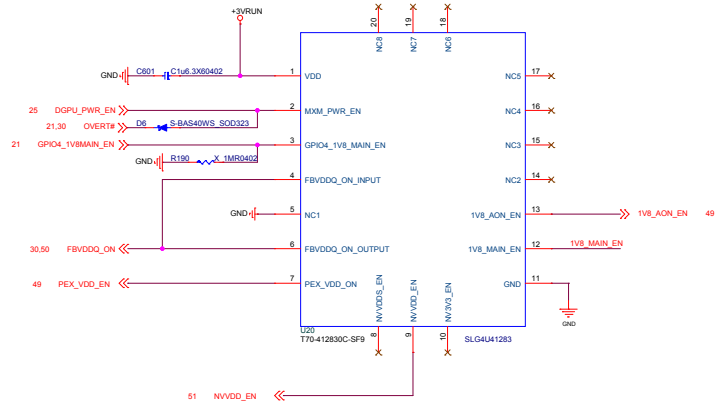
## DGPU POWER GOOD



## Discharge

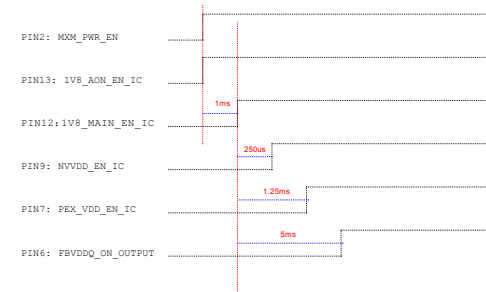


## Power Sequence Control

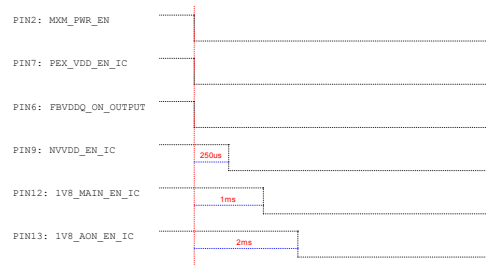


PIN2: MXM\_PWR\_EN is 3.3V INPUT  
 PIN3: GPIO4\_GC6\_PWR\_EN is 1.8V INPUT  
 PIN4: FBVDDQ\_ON\_INPUT 3.3V INPUT  
 PIN6: FBVDDQ\_ON\_OUTPUT 3.3V OUTPUT  
 PIN7: PEX\_VDD\_EN IC 3.3V OUTPUT  
 PIN9: NVVDD\_EN IC 3.3V OUTPUT  
 PIN12: 1V8\_MAIN\_EN IC 3.3V OUTPUT  
 PIN13: 1V8\_AON\_EN\_IC 3.3V OUTPUT

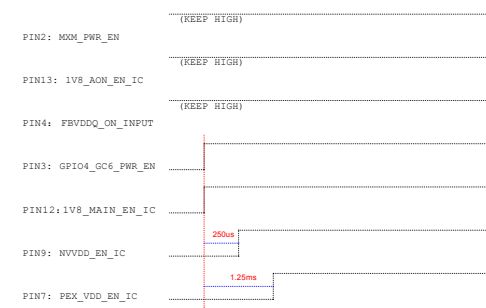
## Power Up Sequence



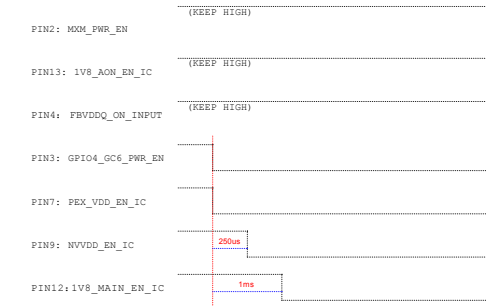
## Power Down Sequence



## GC6 2.1 Exit Sequence

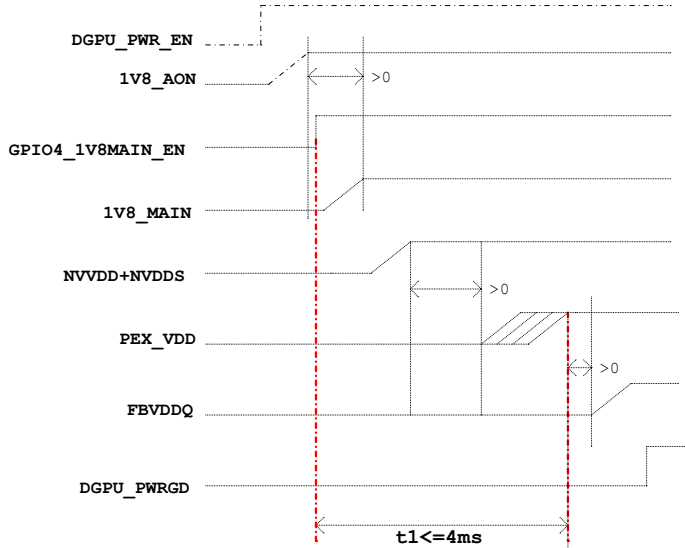


## GC6 2.1 Entry Sequence



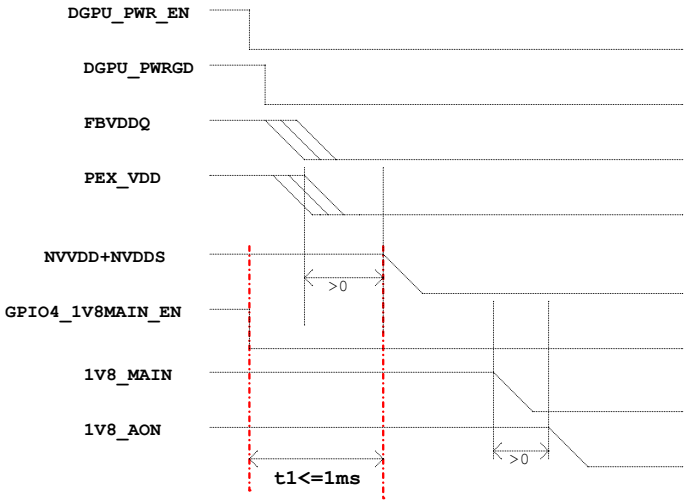
POWER UP Sequence

1V8\_AON -> 1V8\_MAIN->NV3V3 -> NVVDD -> NVVDDS / PEX\_VDD -> FBVDDQ

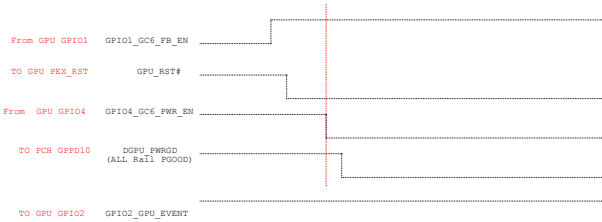


POWER Down Sequence

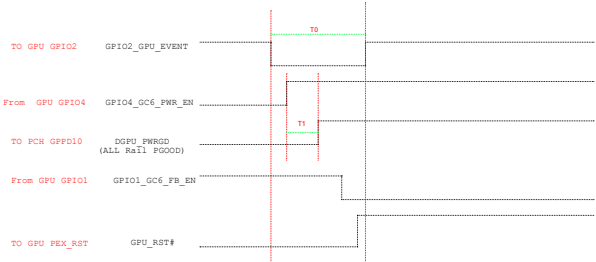
NVVDDS/PEX\_VDD/FBVDDQ ->NVVDD/NV3V3->1V8\_MAIN> 1V8\_AON



GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE

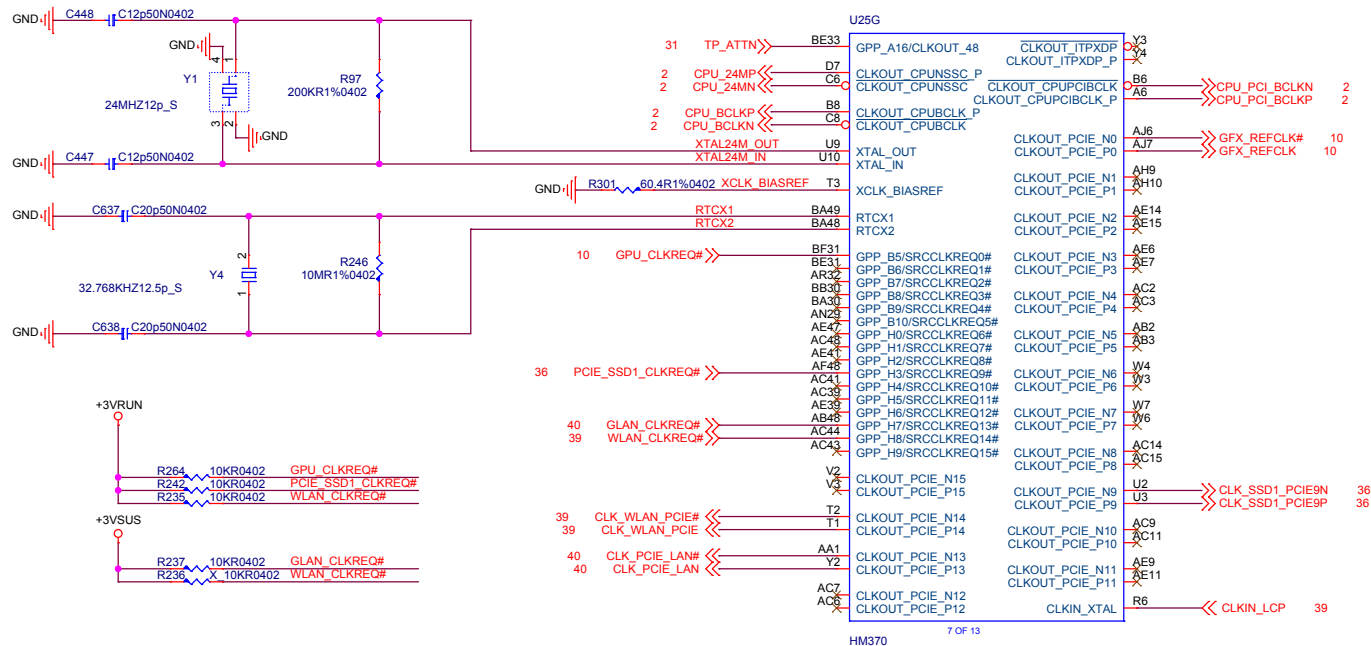


GC6 2.1 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU EVENT# assertion
T1	0.04	4	mS	3V3 MAIN_EN assertion to all power rails up and stable

- NOTES:
- ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
  - During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
  - All delays should be minimized to increase time spent in GC6 for maximum power saving.
  - The entire entry and exit sequence must complete within 200 ms.

# HM370 (RTC/PCIE\_Clock/Clock/RSVD)



## Functional Strap Definitions

### DDPB\_CTRLDATA / GPP\_I6

This signal has a weak internal pull-down.  
0 = Port B is not detected. (Default)  
1 = Port B is detected.

### DDPC\_CTRLDATA / GPP\_I8

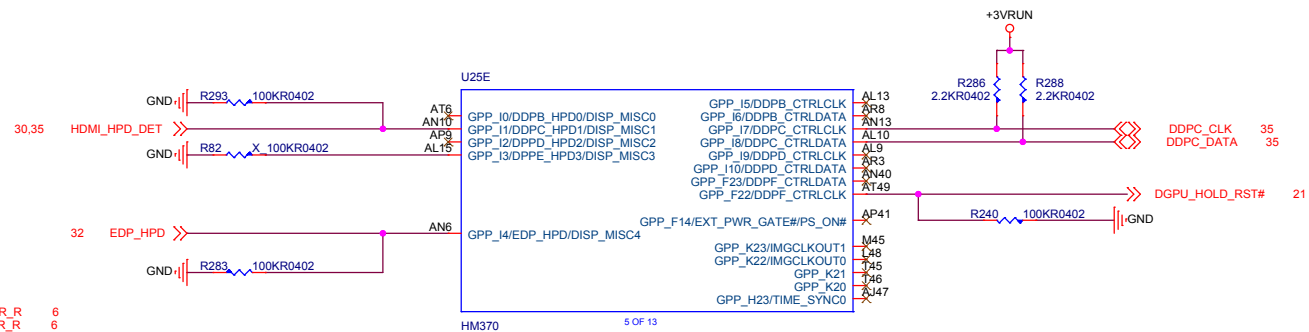
This signal has a weak internal pull-down.  
0 = Port B is not detected. (Default)  
1 = Port B is detected.

### DDPD\_CTRLDATA / GPP\_I10

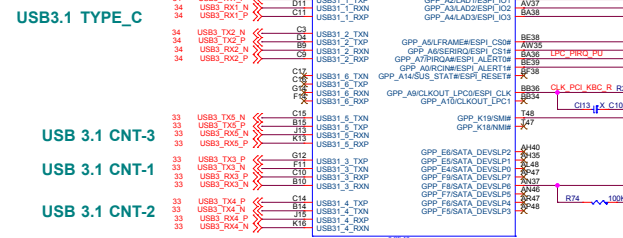
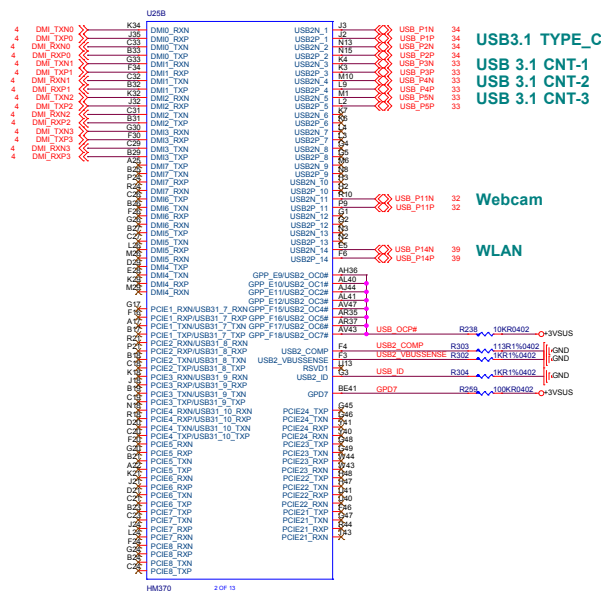
This signal has a weak internal pull-down.  
0 = Port B is not detected. (Default)  
1 = Port B is detected.

### GPP\_F23

This signal has a weak internal pull-down.  
0 = Port F is not detected. (Default)  
1 = Port F is detected.



**HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)**

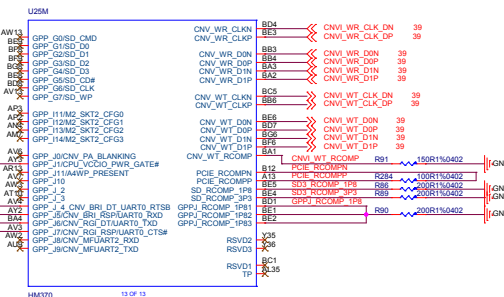
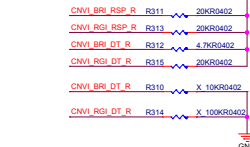
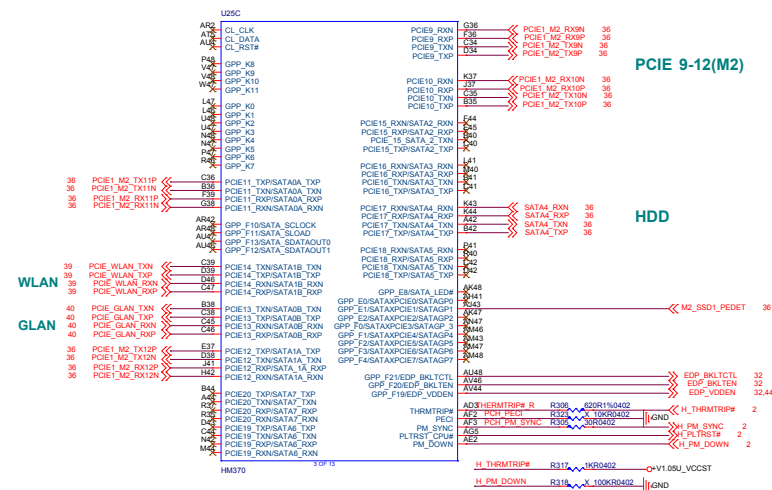


USB			
USB 2.0	USB 3.1	Device	Note
1	1	USB TYPE_C-1	
2	3	USB TYPE_C-2	
3	3	USB TYPE_A-1	
4	4	USB TYPE_A-2	
5	5	USB TYPE_A-3	
6			
7			
8			
9			
10			
11		WebCam	
12			
13			
14		WLAN	

**GPD7**  
External pull-up is required. Recommend 100K.  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

High Speed I/O Ports				
		FM370	Device	
1	USB3.1 Gen 1		NC	
2	USB3.1 Gen 1		NC	
3	N/A		NC	
4	N/A		NC	
5	INTEL LAN Only		NC	
6	N/A		NC	
7	N/A		NC	
8	N/A		NC	
9	PCIe/LAN	PICE Configurable M.2	M.2 SSD-1	
10	PCIe			
11	PCIe/SATA0A			
12	PCIe/LAN/SATA1A			
13	PCIe/LAN/SATA0B			LAN
14	PCIe/SATA1B			WLAN
15	PCIe			NC
16	PCIe			NC
17	PCIe/SATA4		HDD	
18	PCIe/SATA5		NC	
19	PCIe		NC	
20	PCIe		NC	
21	PCIe		NC	
22	PCIe			
23	PCIe			
24	PCIe			

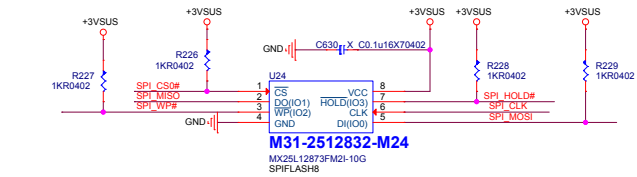
SATA Lane 0 has the flexibility to be mapped to PCIE 11 or 13  
SATA Lane 1 has the flexibility to be mapped to PCIE 12 or 14







**SPI FLASH ROM      16MB**



PLT\_RST#

U7A

NC7WZ17P6X\_NL\_SC70-6

JNC6

M2\_SSD\_RST#

LPC\_RST#

U7B

NC7WZ17P6X\_NL\_SC70-6

JNC2

JNC3

JNC5

WLAN\_RST#

LAN\_RST#

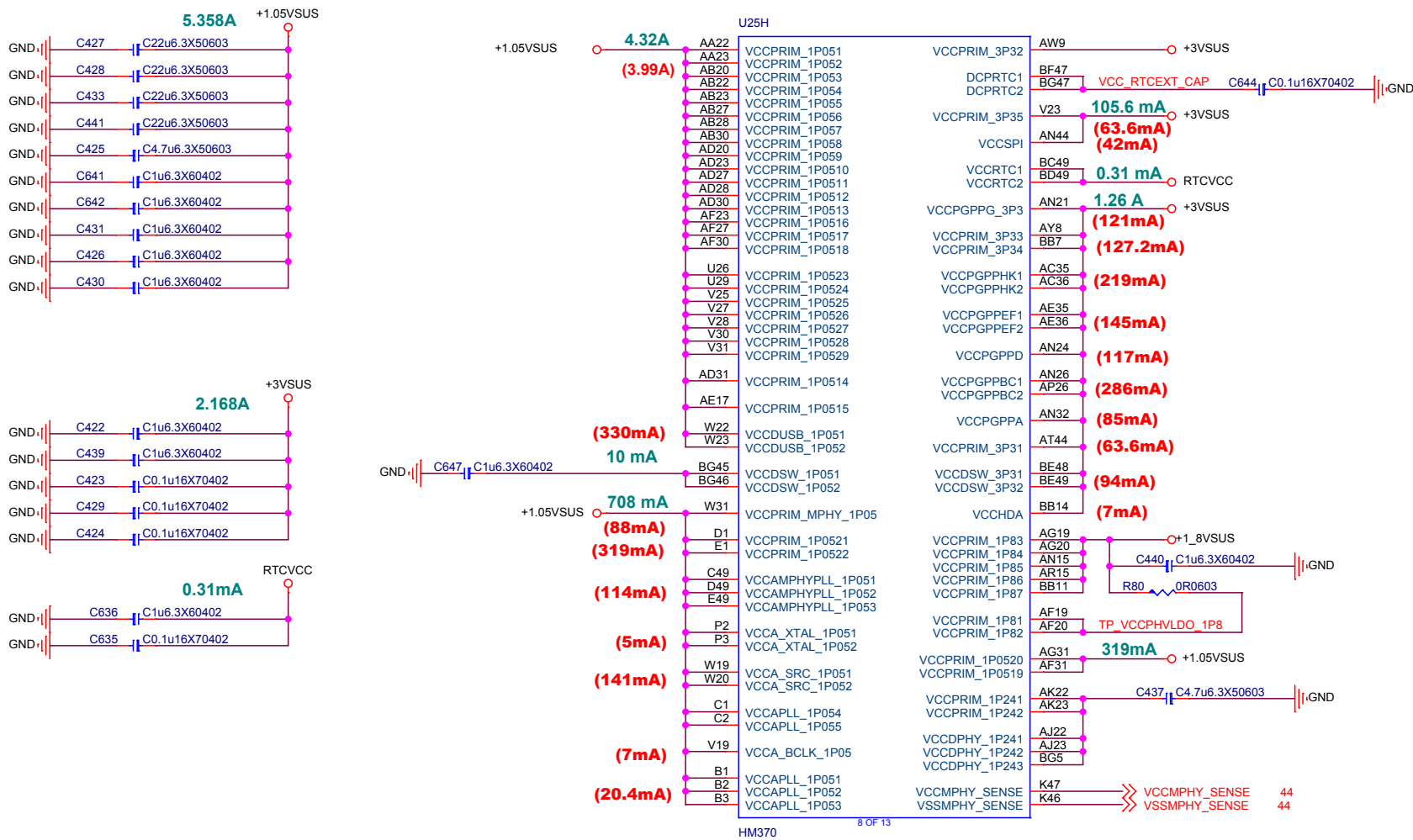
PEG\_RST#

R76

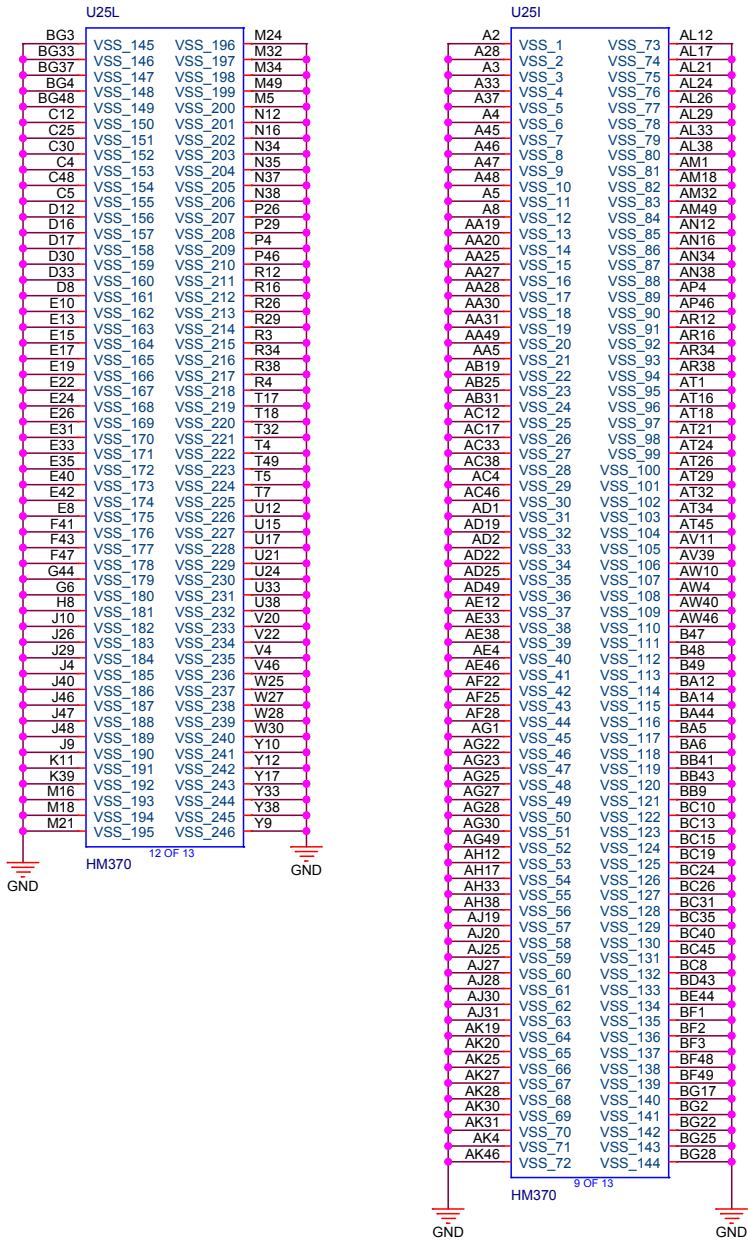
100kR0402



# HM370 (Power)

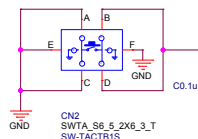


# PCH-H(GND)

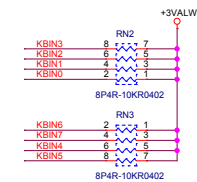
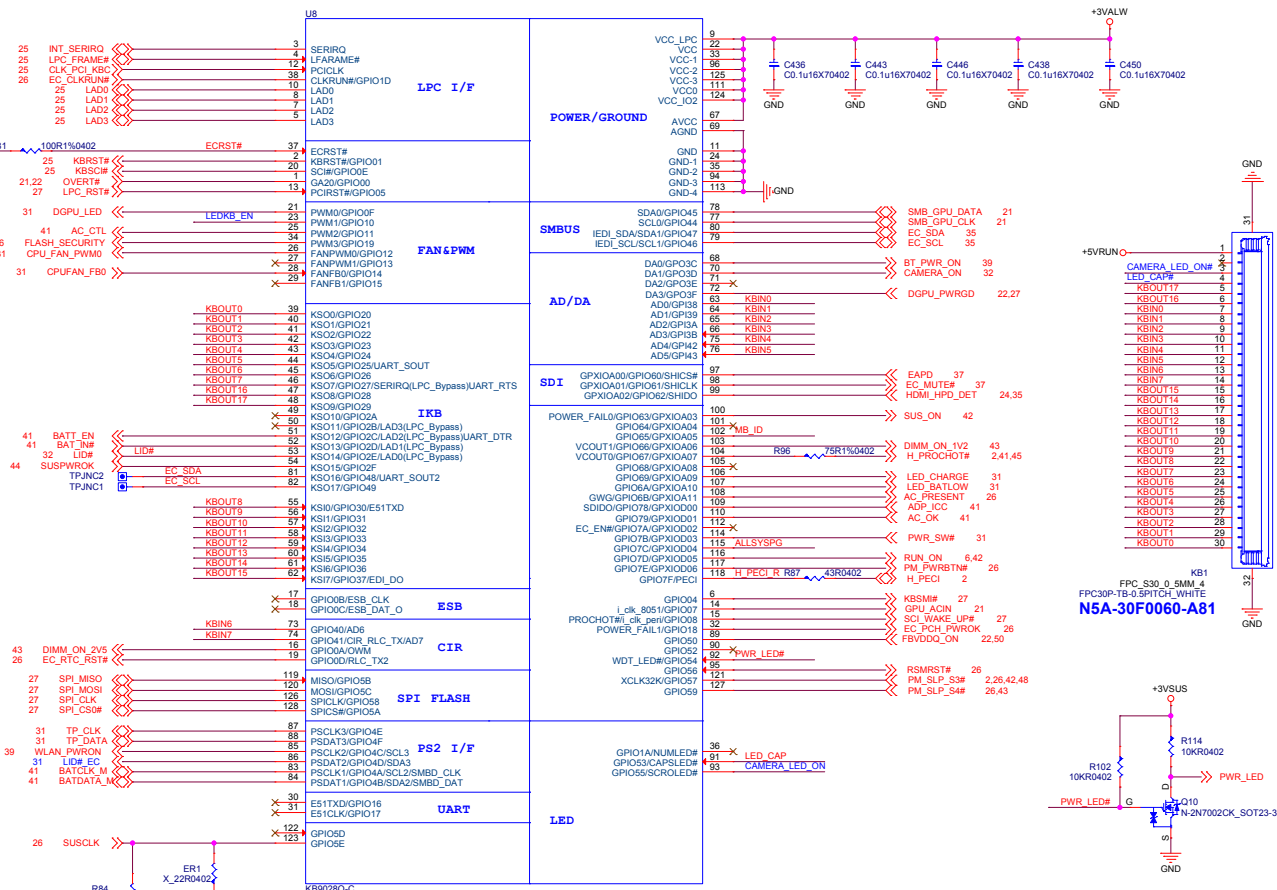


<b>msi</b> MICRO-STAR INT'L CO.,LTD.			
Title <b>PCH-6(GND)</b>			
Size	Document	Number	Rev
Custom	<b>MS-16R1</b>		<b>1.0</b>
Date:	Wednesday, April 11, 2018		
Sheet	29 of 57		

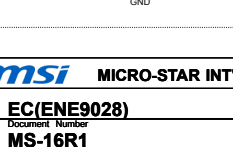
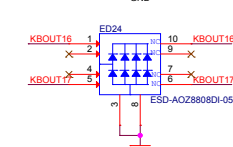
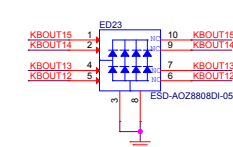
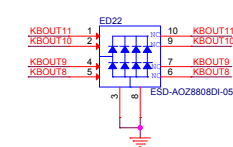
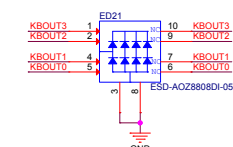
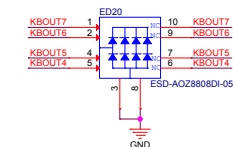
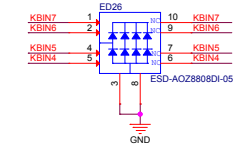
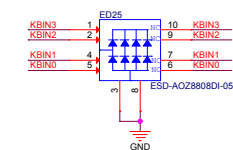
## Hardware Reset



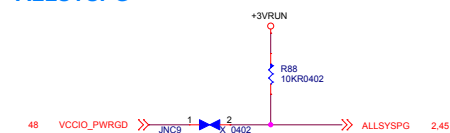
**N71-0101630-D02**



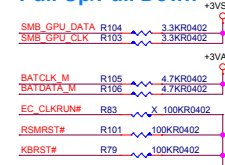
For EM



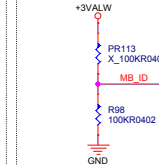
## ALLSYSPG



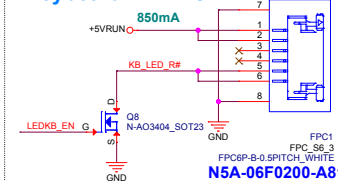
### Pull Up/Pull Down



## MB ID

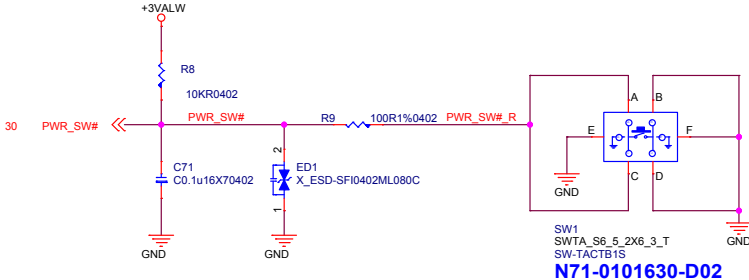


## Keyboard LED CONN

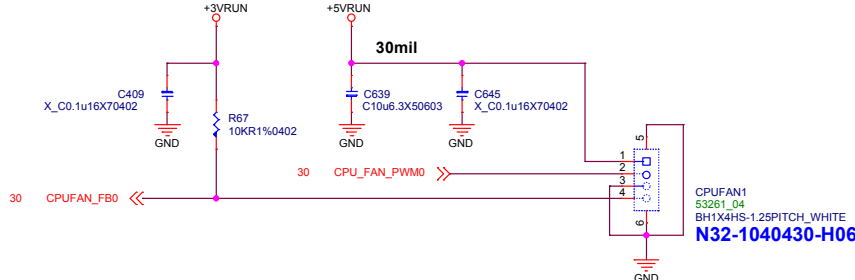


## Power Switch / FAN / Touch Pad / LED

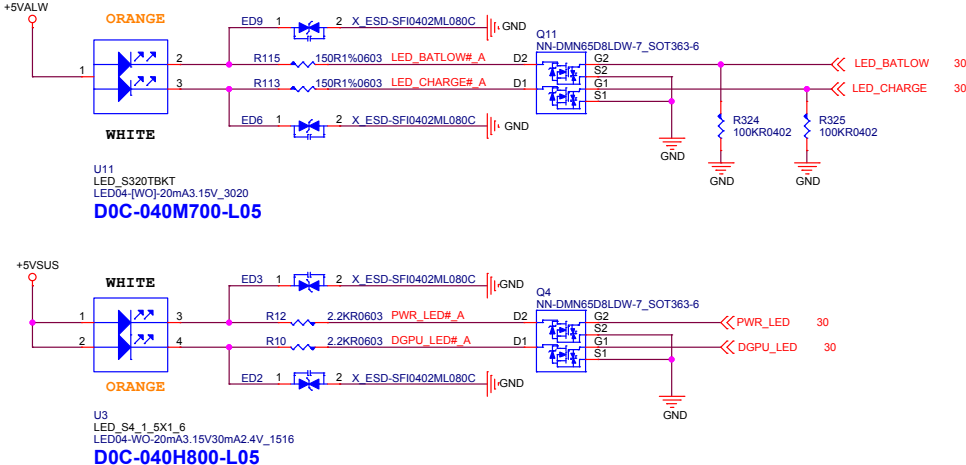
## Power Switch



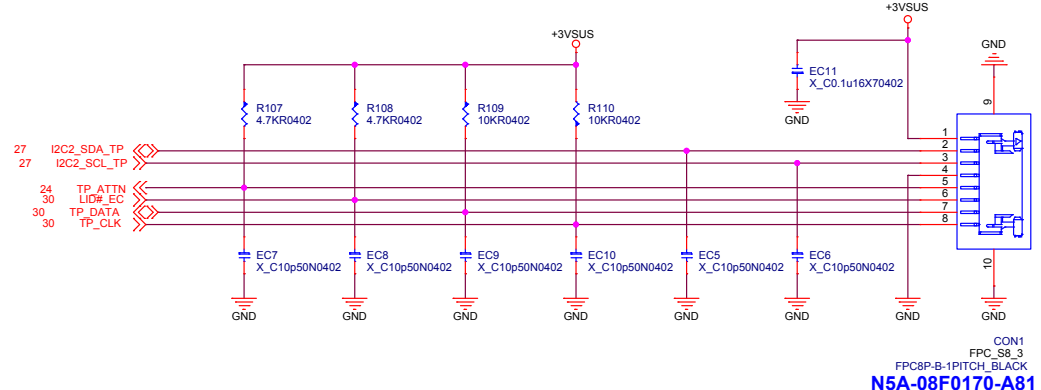
## CPU FAN



## LED

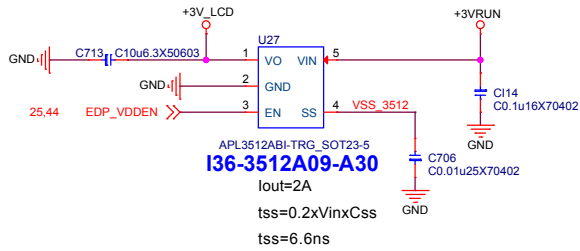


## Touch Pad Board

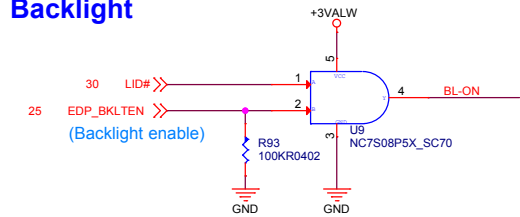


	<b>MICRO-STAR INT'L CO.,LTD.</b>
<b>Title</b>	
<b>Power Switch/FAN/Touch Pad/LED</b>	
<b>Size</b> Custom	<b>Document Number</b> <div style="background-color: black; color: white; padding: 5px; text-align: center; font-weight: bold; font-size: 1.2em;">MS-16R1</div>
<b>Date</b>	Wednesday, April 11, 2018
<b>Sheet</b>	31 of 57

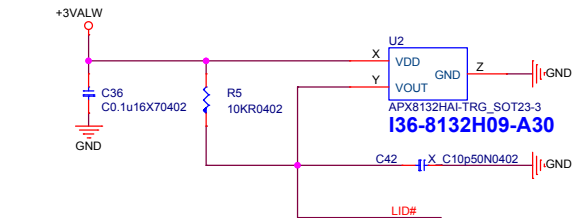
## Pannel Device Logic Power



## Backlight



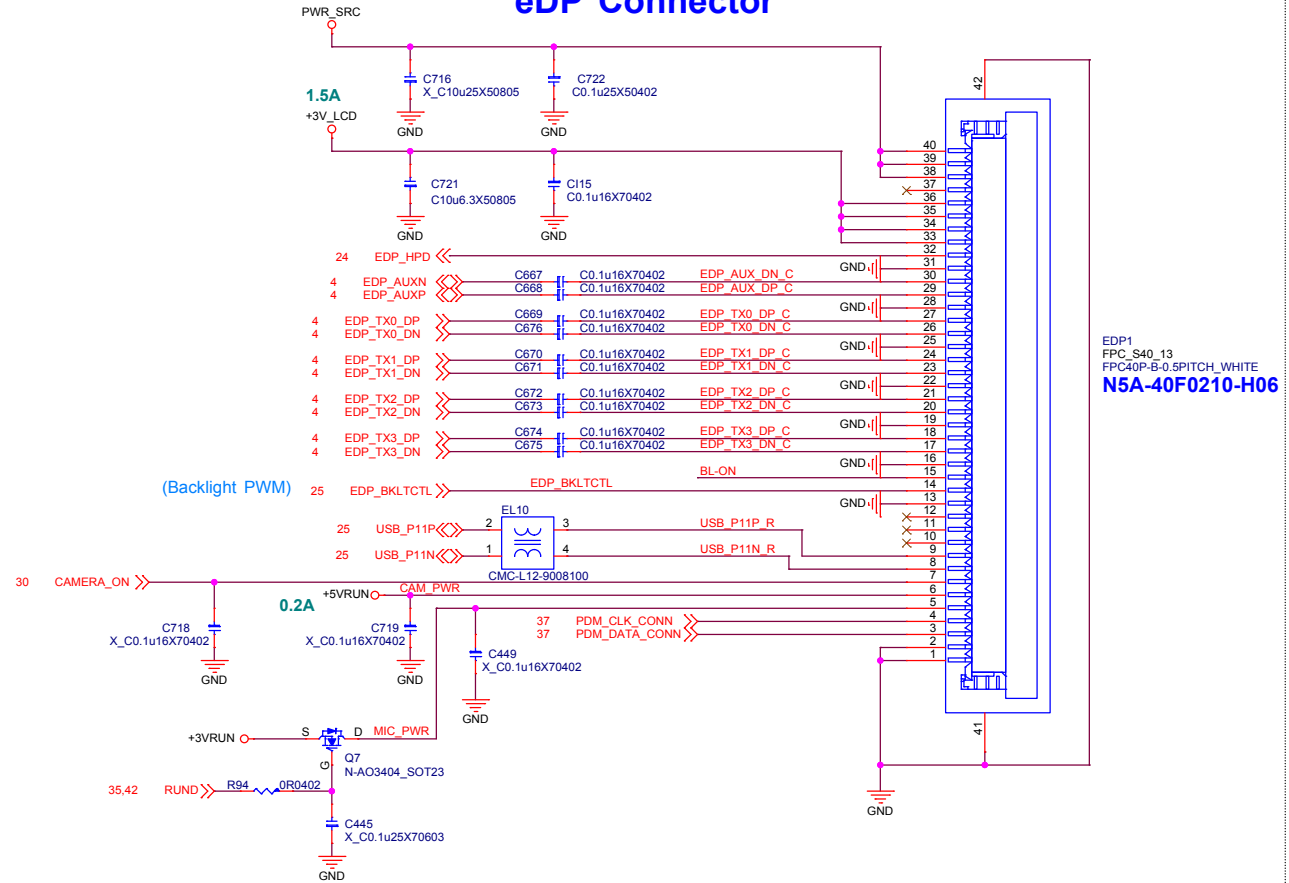
## Hall Switch



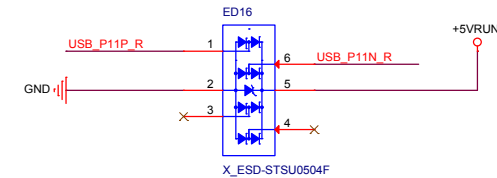
## EMI Close Connector



## eDP Connector

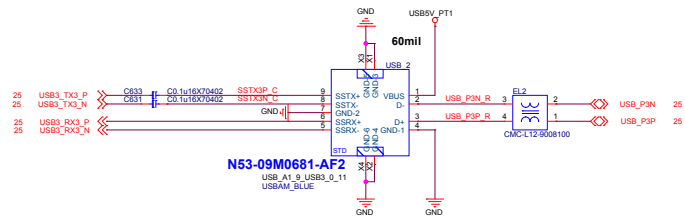


## ESD

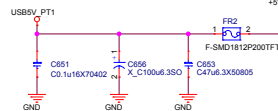




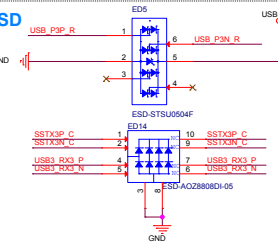
## USB3.0 CNT-1



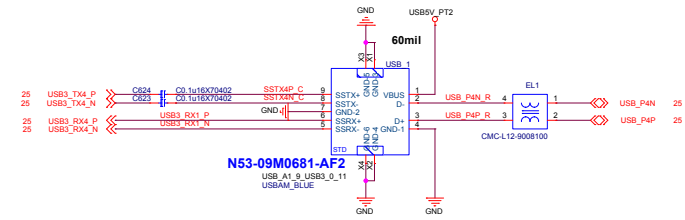
## USB Power Switch



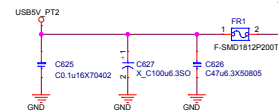
**ESD**



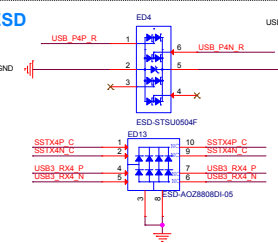
### USB3.0 CNT-2



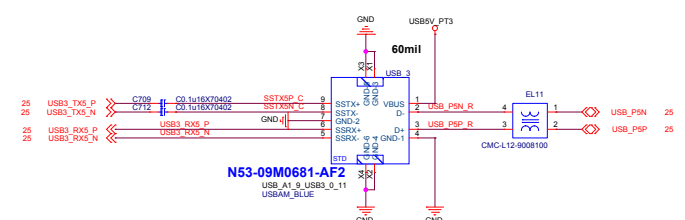
## USB Power Switch



ESD



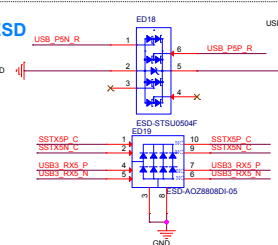
## USB3.0 CNT-3



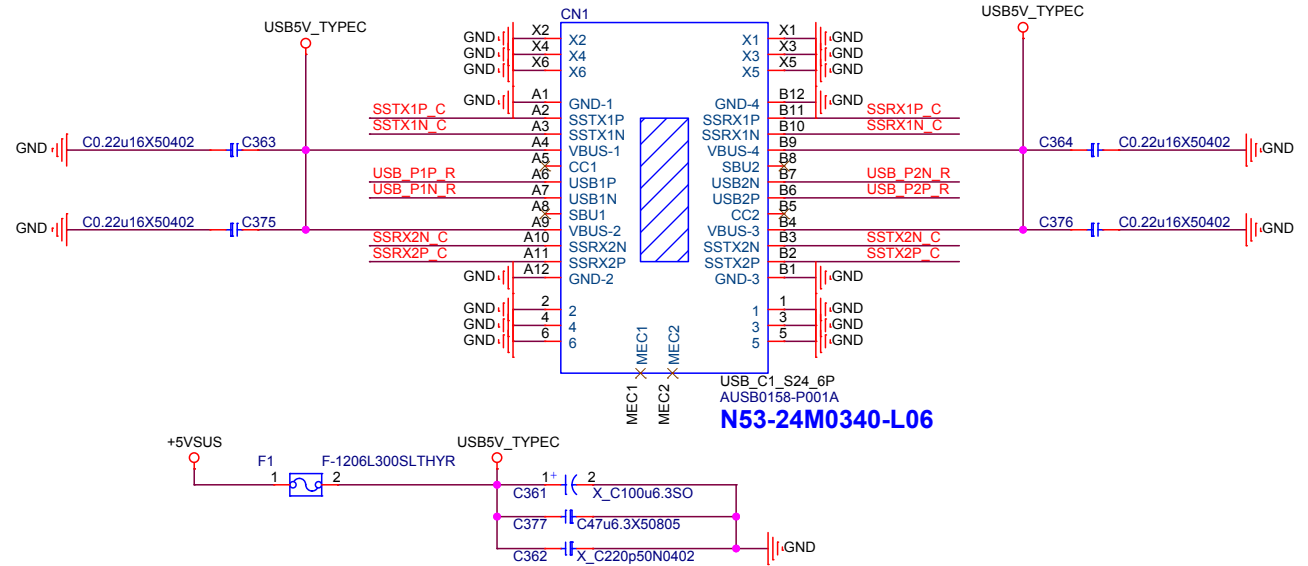
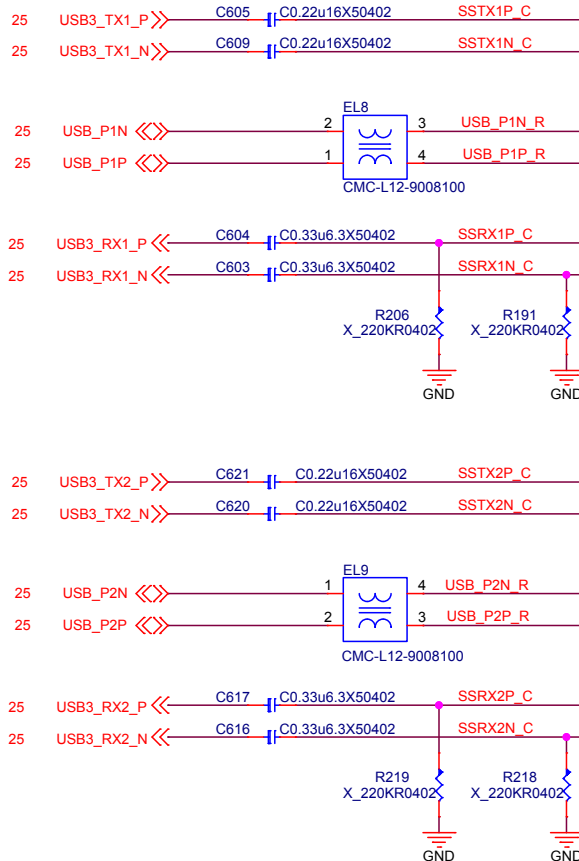
### USB Power Switch



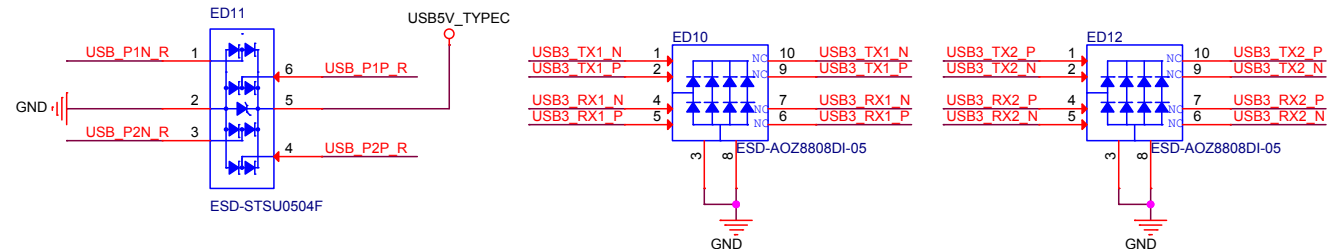
ESD




# USB 3.0 TYPE\_C

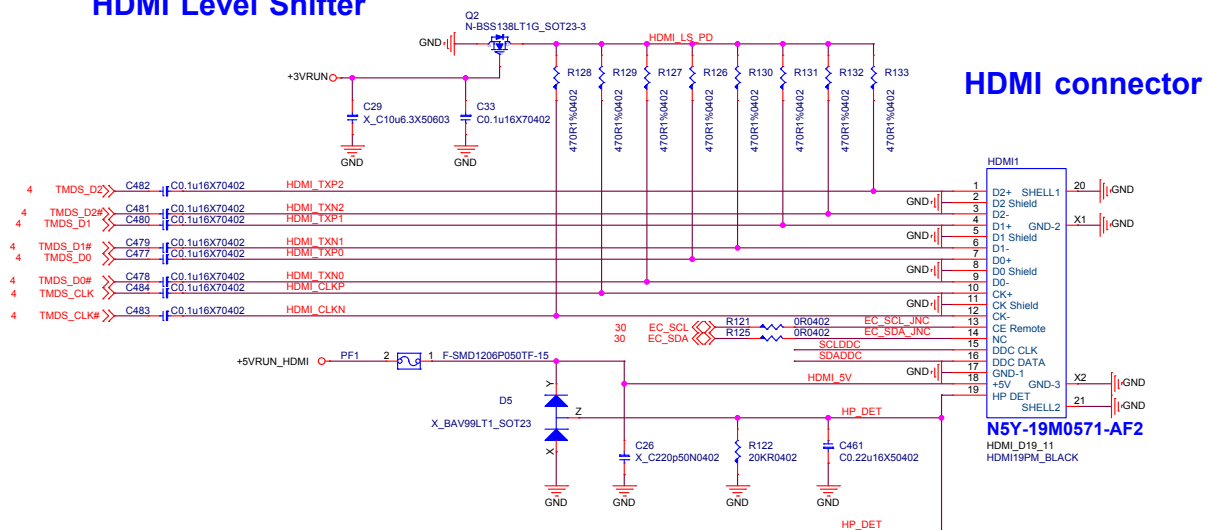


## ESD

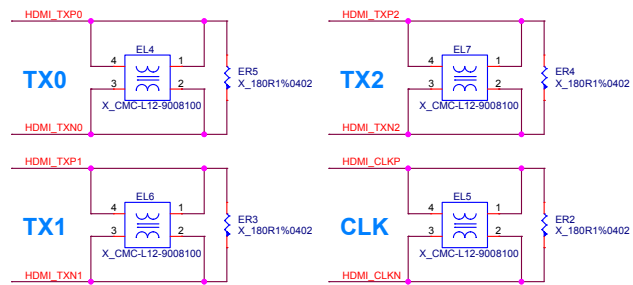


		MICRO-STAR INT'L CO.,LTD.	
Title			
USB 3.0 TYPE_C			
Size	Document Number		Rev
Custom	MS-16R1		1.0
Date:	Wednesday, April 11, 2018	Sheet	34 of 57

# HDMI Level Shifter

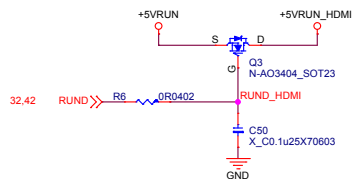


## EMI Close Connector

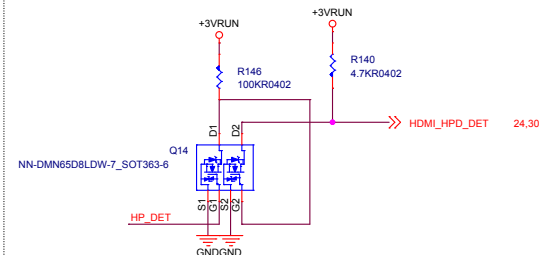


## Avoid HDMI Leakage

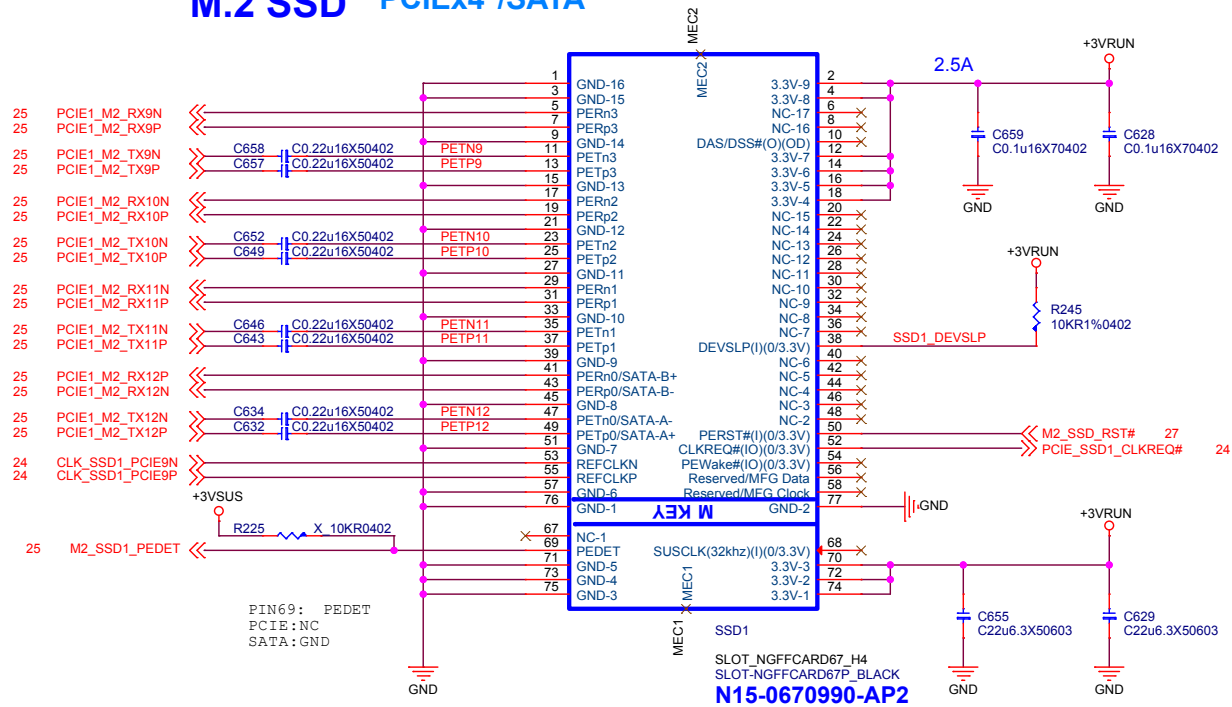
W>20mils



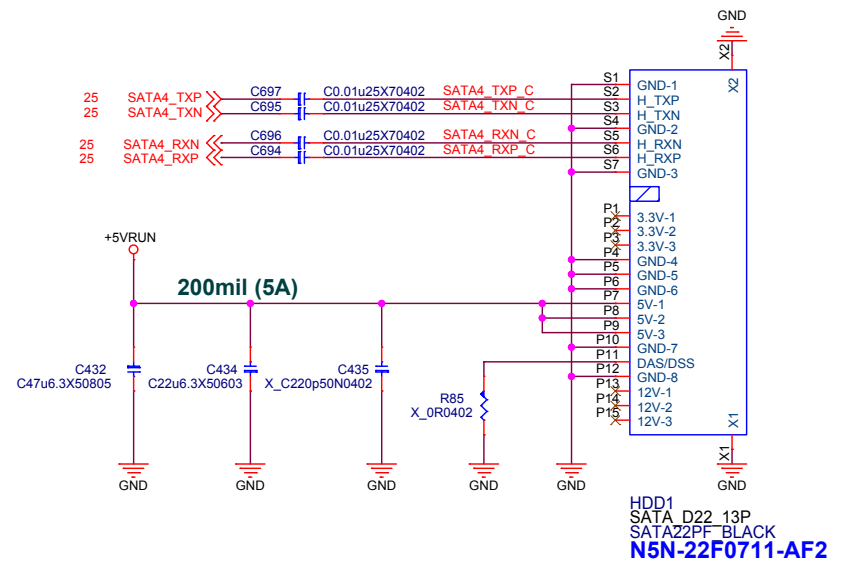
## HPD Level Shift 5V to 3V for Debug Card



**M.2 SSD**    **PCIEx4 /SATA**



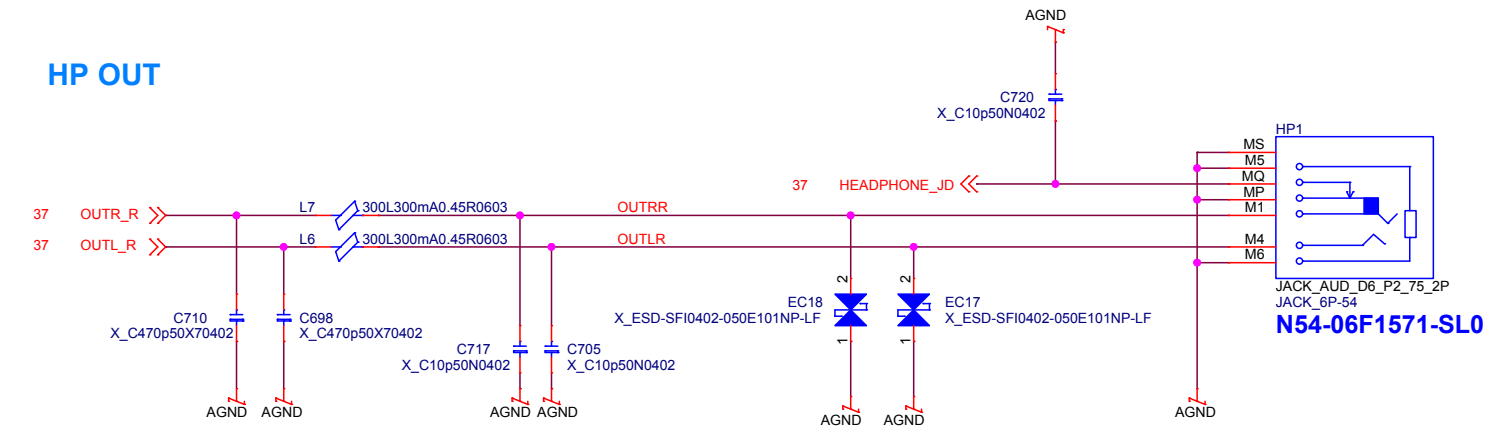
## HDD



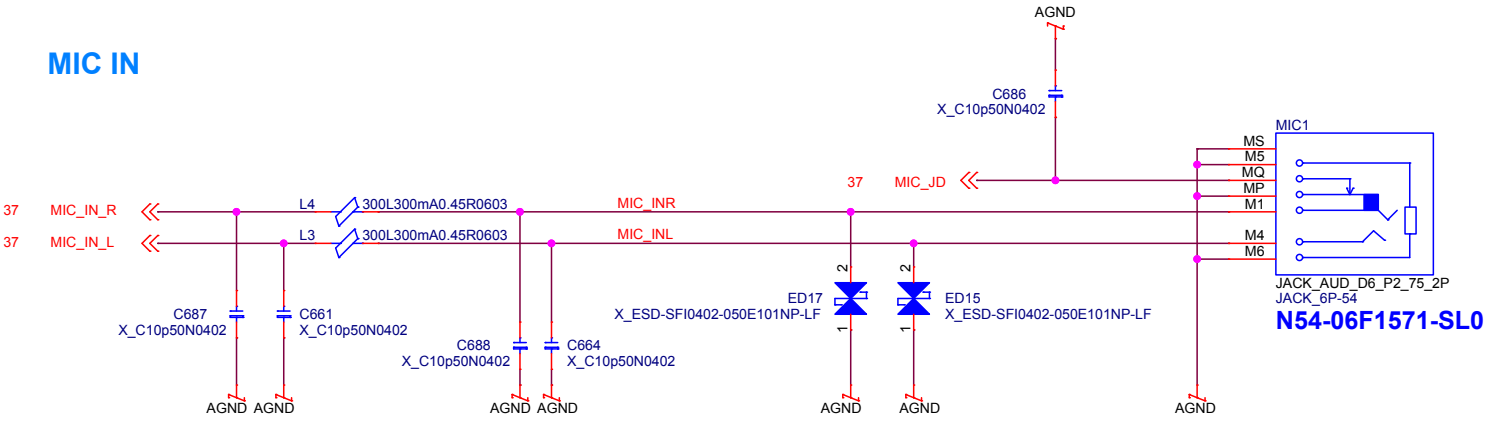


# Audio CONN

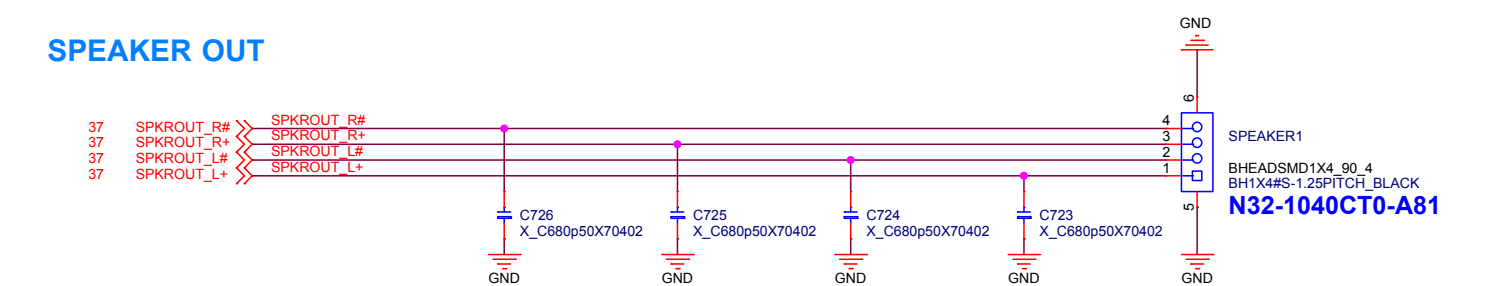
## HP OUT



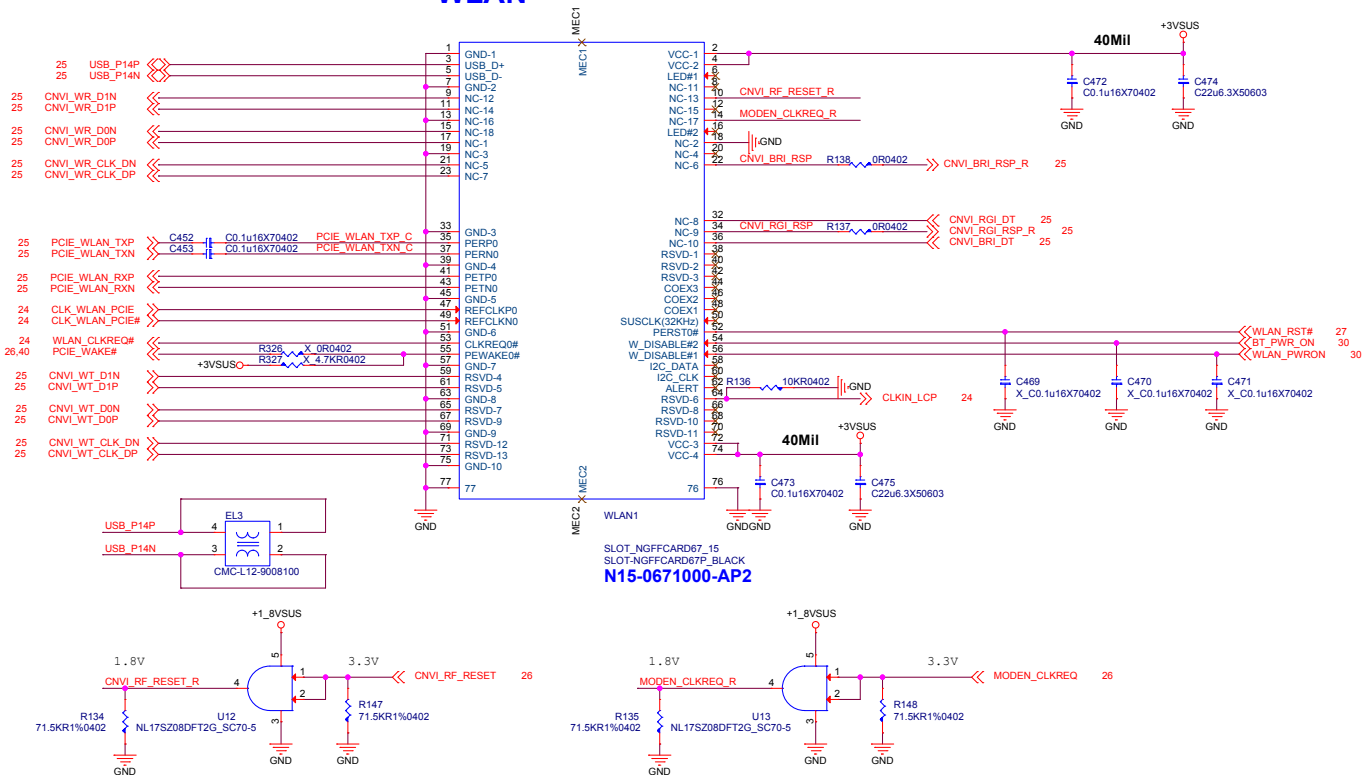
## MIC IN



## SPEAKER OUT



## WLAN



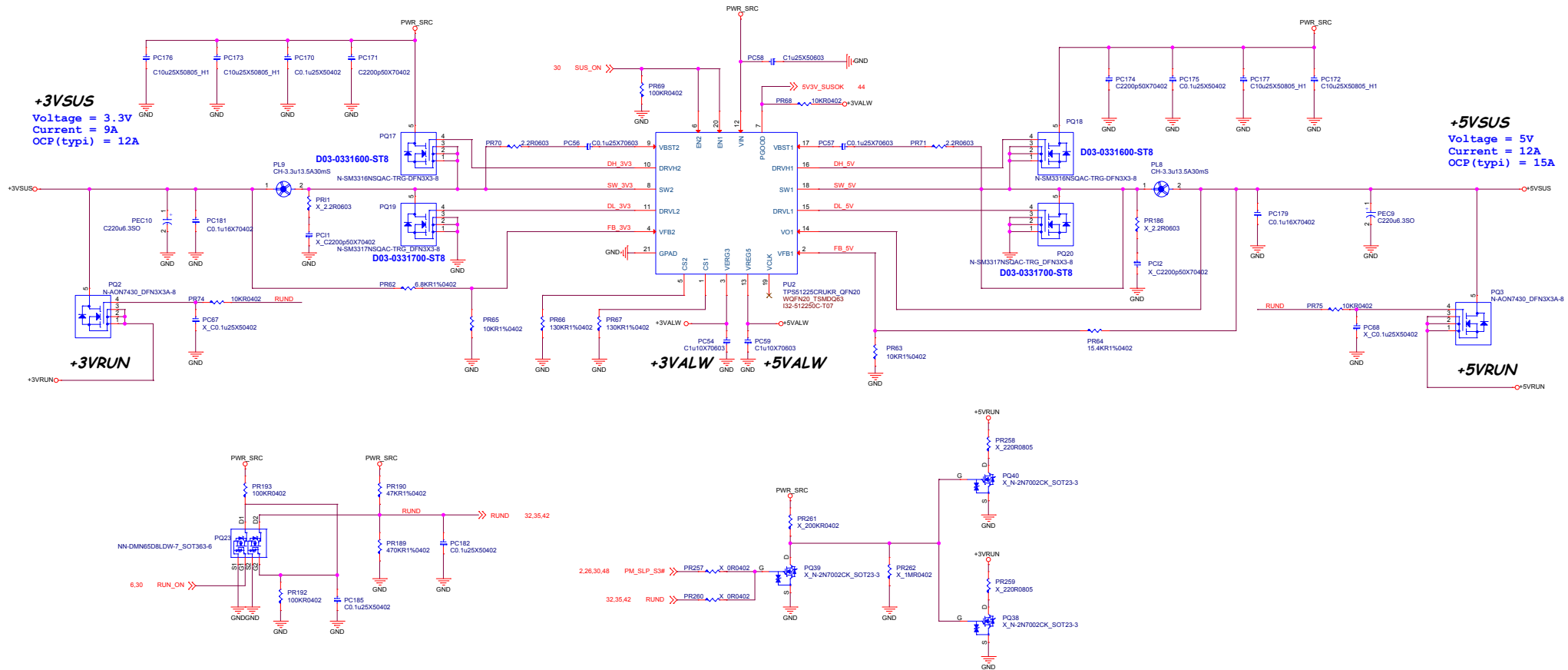
Pin #	M.2 WLAN	INTEL CNVI WLAN	Pin #	M.2 WLAN	INTEL CNVI WLAN
Pin 1	GND	GND	Pin 2	3.3V	3.3V
Pin 3	USB_D+	N/C	Pin 4	3.3V	3.3V
Pin 5	USB_D-	N/C	Pin 6	LED1#	LED1#
Pin 7	GND	GND	Pin 8	Module Key	N/C
Pin 9	Module Key	WGR_D1N	Pin 10	Module Key	RF_RESET_B(1.8V)
Pin 11	Module Key	WGR_D1P	Pin 12	Module Key	N/C
Pin 13	Module Key	GND	Pin 14	Module Key	CLKREQ0(1.8V)
Pin 15	Module Key	WGR_D0N	Pin 16	LED2#	LED2#
Pin 17	N/C	WGR_D0P	Pin 18	GND	GND
Pin 19	N/C	GND	Pin 20	N/C	N/C
Pin 21	N/C	WGR_CLKN	Pin 22	N/C	BRI_RSP(1.8V)
Pin 23	N/C	WGR_CLKP	Pin 24	Module Key	Module Key
Pin 25	Module Key	Module Key	Pin 26	Module Key	Module Key
Pin 27	Module Key	Module Key	Pin 28	Module Key	Module Key
Pin 29	Module Key	Module Key	Pin 30	Module Key	Module Key
Pin 31	Module Key	Module Key	Pin 32	N/C	RGI_DT(1.8V)
Pin 33	GND	GND	Pin 34	N/C	RGI_RSP(1.8V)
Pin 35	PERP0	N/C	Pin 36	N/C	BGI_DT(1.8V)
Pin 37	PERN0	N/C	Pin 38	N/C	N/C
Pin 39	GND	GND	Pin 40	N/C	N/C
Pin 41	PETP0	N/C	Pin 42	N/C	N/C
Pin 43	PETN0	N/C	Pin 44	N/C	N/C
Pin 45	GND	GND	Pin 46	N/C	N/C
Pin 47	REFCLKP0	N/C	Pin 48	N/C	N/C
Pin 49	REFCLKN0	N/C	Pin 50	SUSCLK (32KHz)	SUSCLK (32KHz)
Pin 51	GND	GND	Pin 52	PERST0#	N/C
Pin 53	CLKREQ0#	N/C	Pin 54	BT_EN (W_DISABLE2#)	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	N/C	Pin 56	WLAN_EN (W_DISABLE2#)	WLAN_EN (W_DISABLE2#)
Pin 57	GND	GND	Pin 58	N/C	N/C
Pin 59	N/C	WT_D1N	Pin 60	N/C	N/C
Pin 61	N/C	WT_D1P	Pin 62	N/C	N/C
Pin 63	GND	GND	Pin 64	Resever	REFCLK0(38.4MKz)
Pin 65	N/C	WT_D0N	Pin 66	N/C	N/C
Pin 67	N/C	WT_D0P	Pin 68	N/C	N/C
Pin 69	GND	GND	Pin 70	N/C	N/C
Pin 71	N/C	WT_CLKN	Pin 72	3.3V	3.3V
Pin 73	N/C	WT_CLKP	Pin 74	3.3V	3.3V
Pin 75	GND	GND			



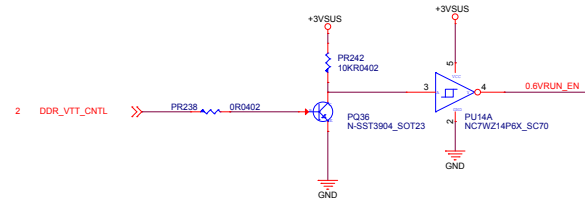
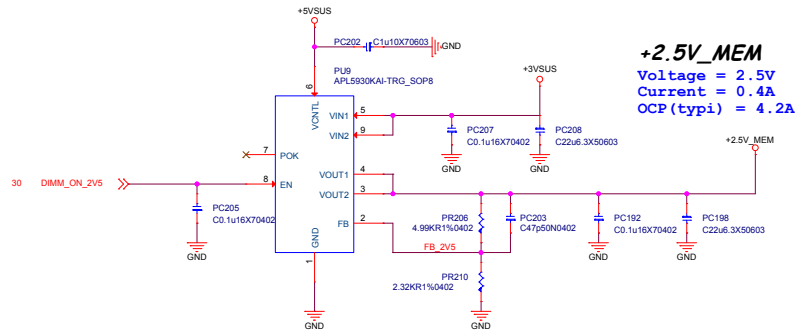




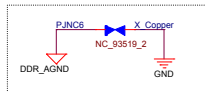
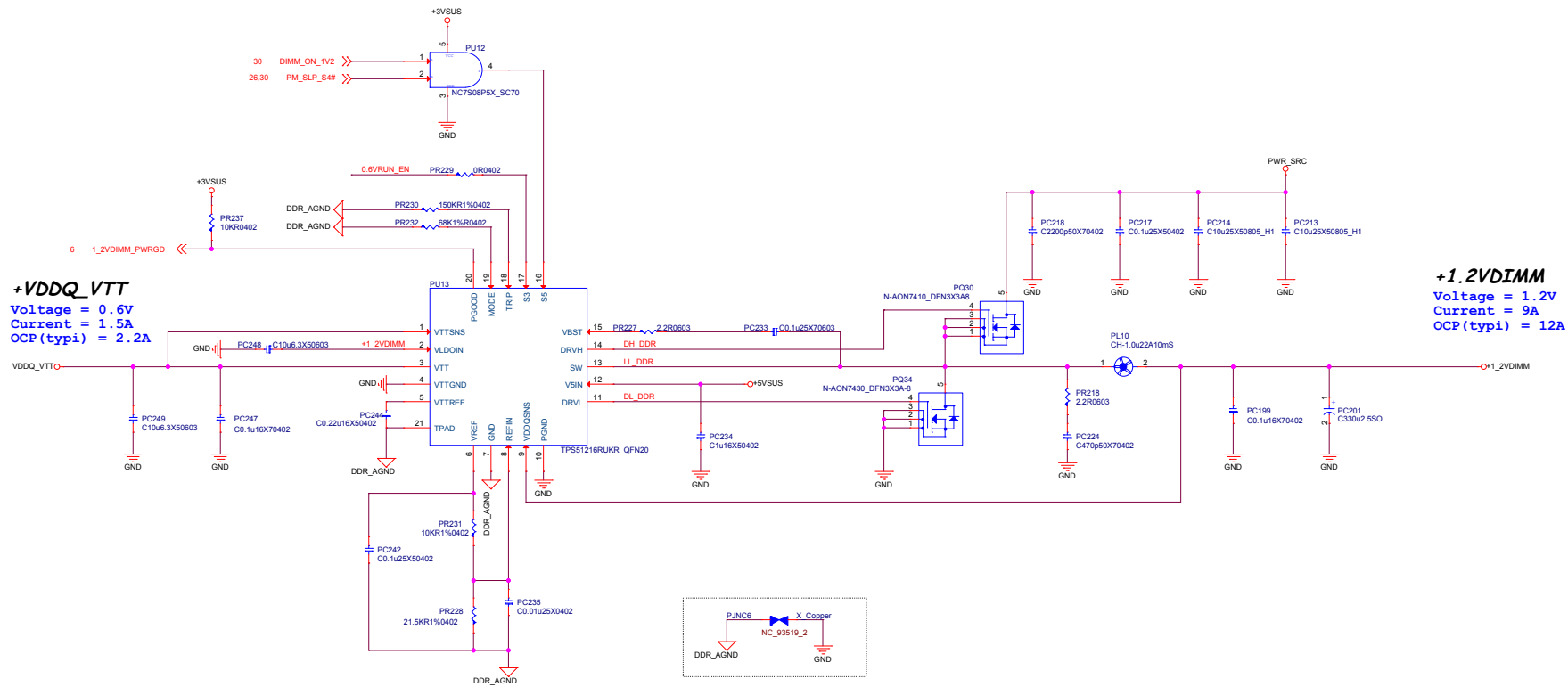
## System Power



## +2.5V\_MEM

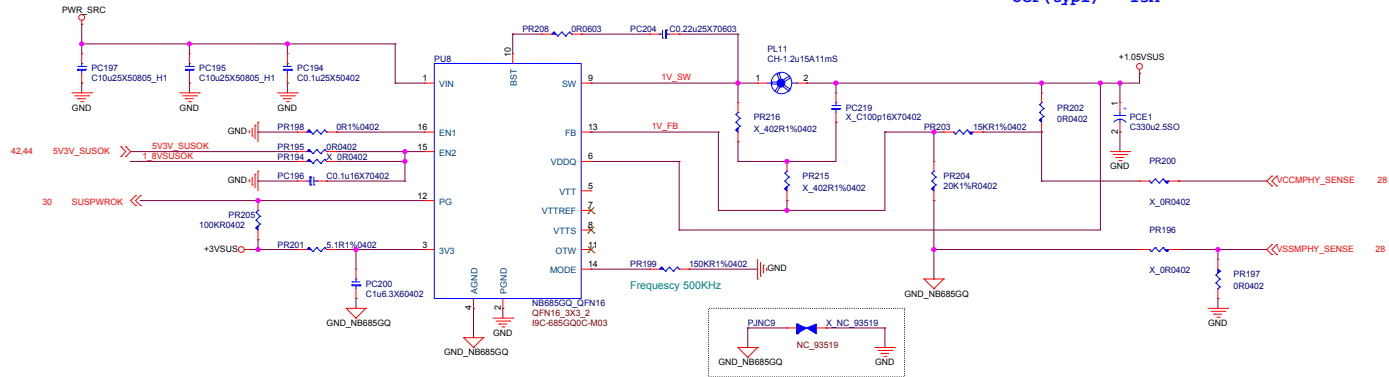


## +1.2VDIMM / VDDQ\_VTT(0.6V)



**+1.05VSUS**

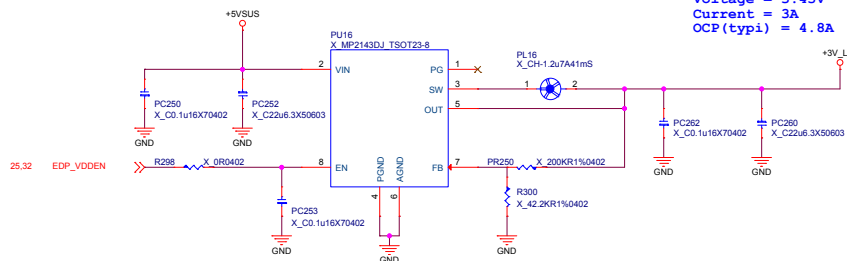
Voltage = 1.05V  
Current = 10A  
OCP(typi) = 13A



**+3V\_LCD**

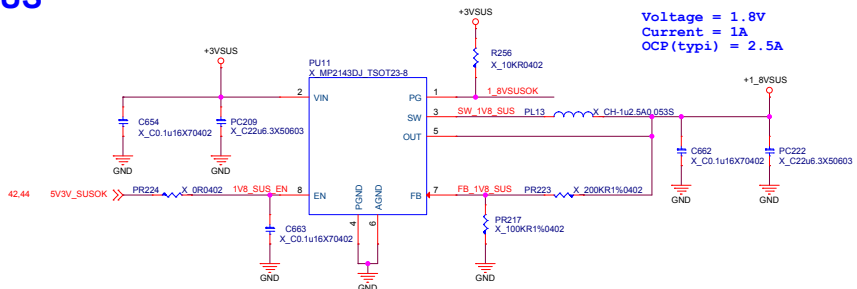
## Pannel Device Logic Power

Voltage = 3.45V  
Current = 3A  
OCP(typi) = 4.8A



**+1\_8VSUS**

Voltage = 1.8V  
Current = 1A  
OCP(typi) = 2.5A

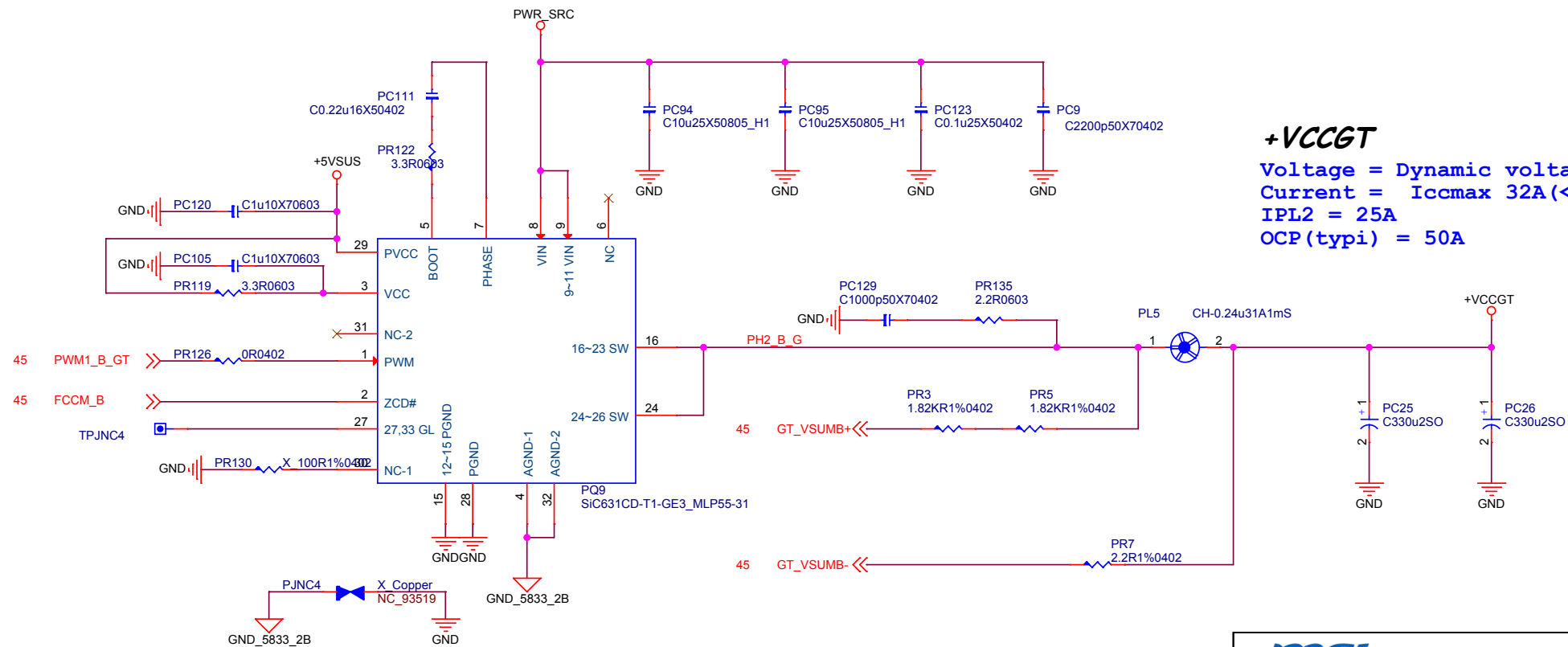









# +VCCGT

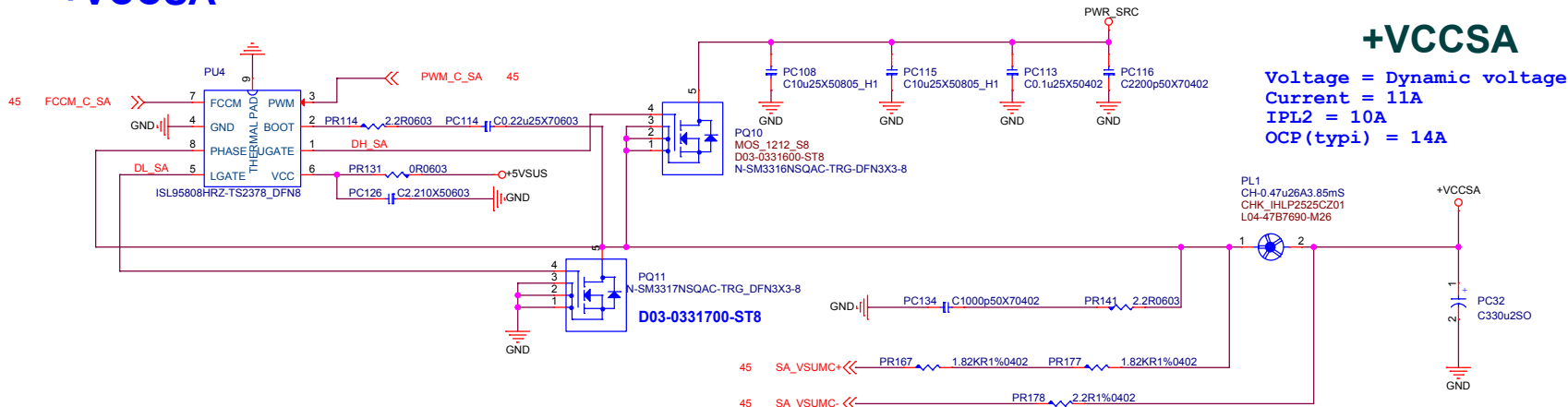


## +VCCGT

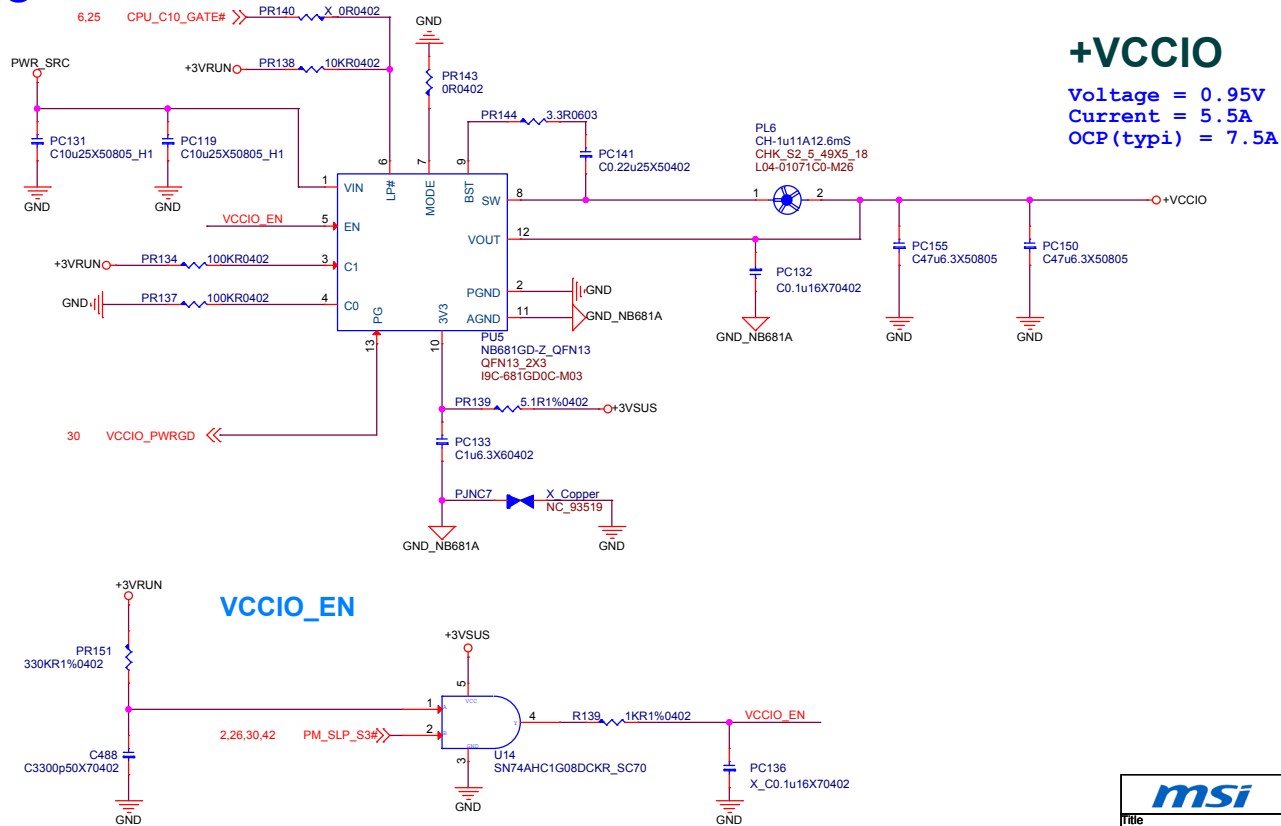
Voltage = Dynamic voltage  
Current = Iccmax 32A(<10ms)  
IPL2 = 25A  
OCP(typi) = 50A

		MICRO-STAR INT'L CO.,LTD.	
Title			
CPU Power (VCCGT)			
Size	Document Number	Rev	
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# +VCCSA

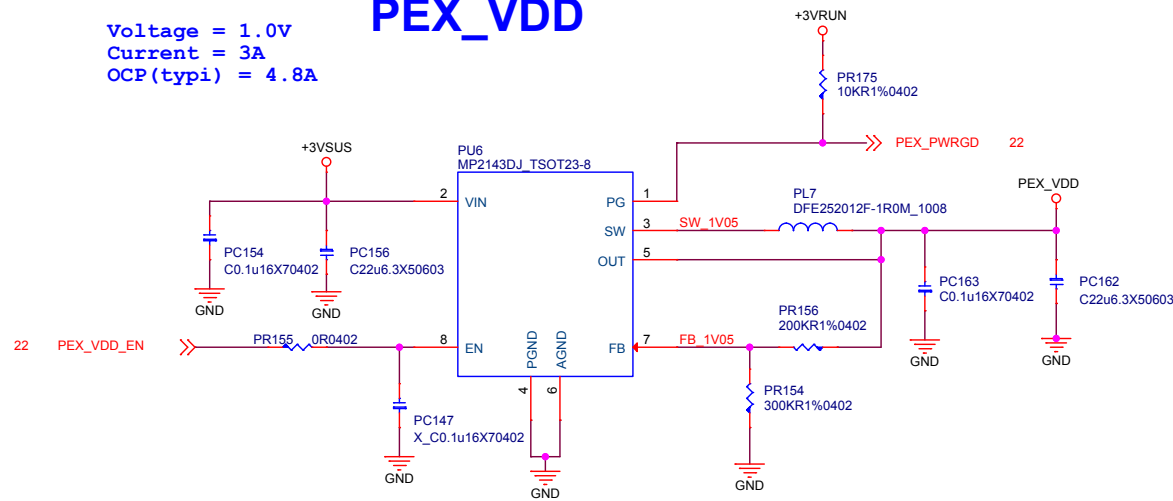


# +VCCIO

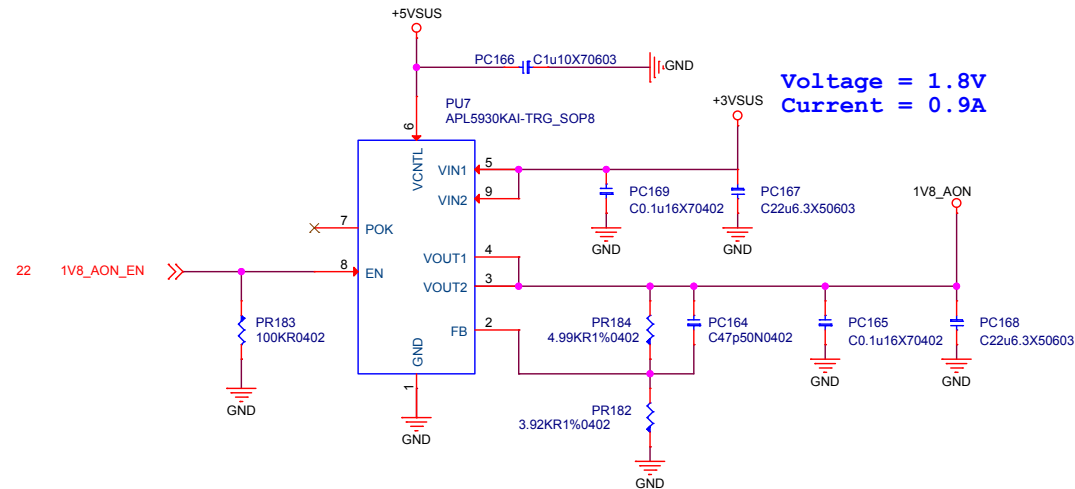



Voltage = 1.0V  
Current = 3A  
OCP(typi) = 4.8A

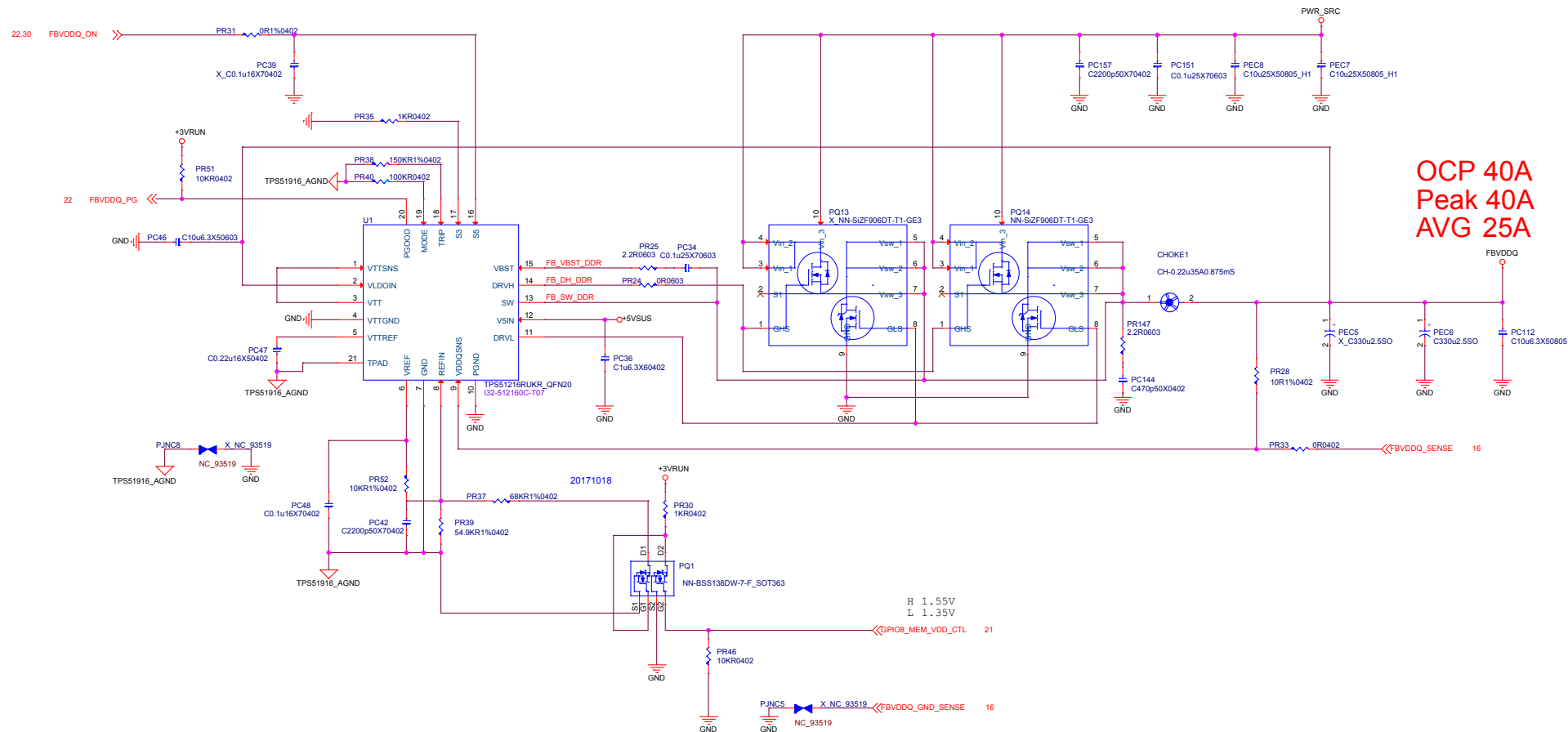
## PEX\_VDD



## 1V8\_AON



		MICRO-STAR INT'L CO.,LTD.	
Title			
DGPU POWER PEX VDD/1V8 AON			
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OCP 40A  
Peak 40A  
AVG 25A

# DGPU POWER / UP9509P

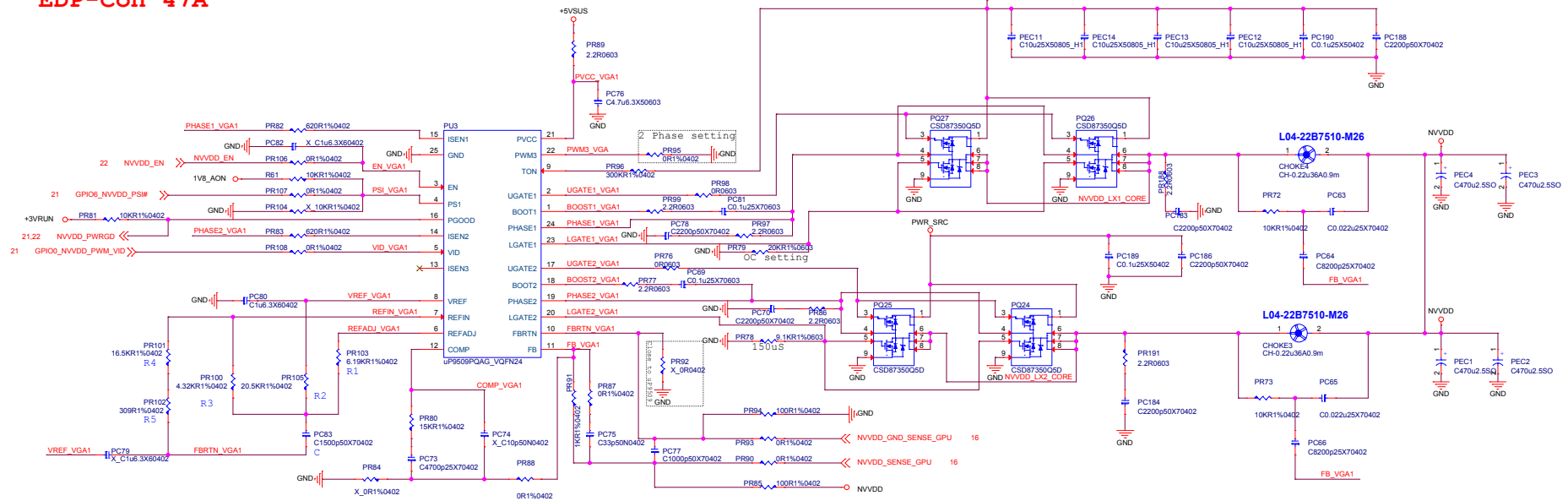
EDP-Peak 90A

EDP-Con 47A

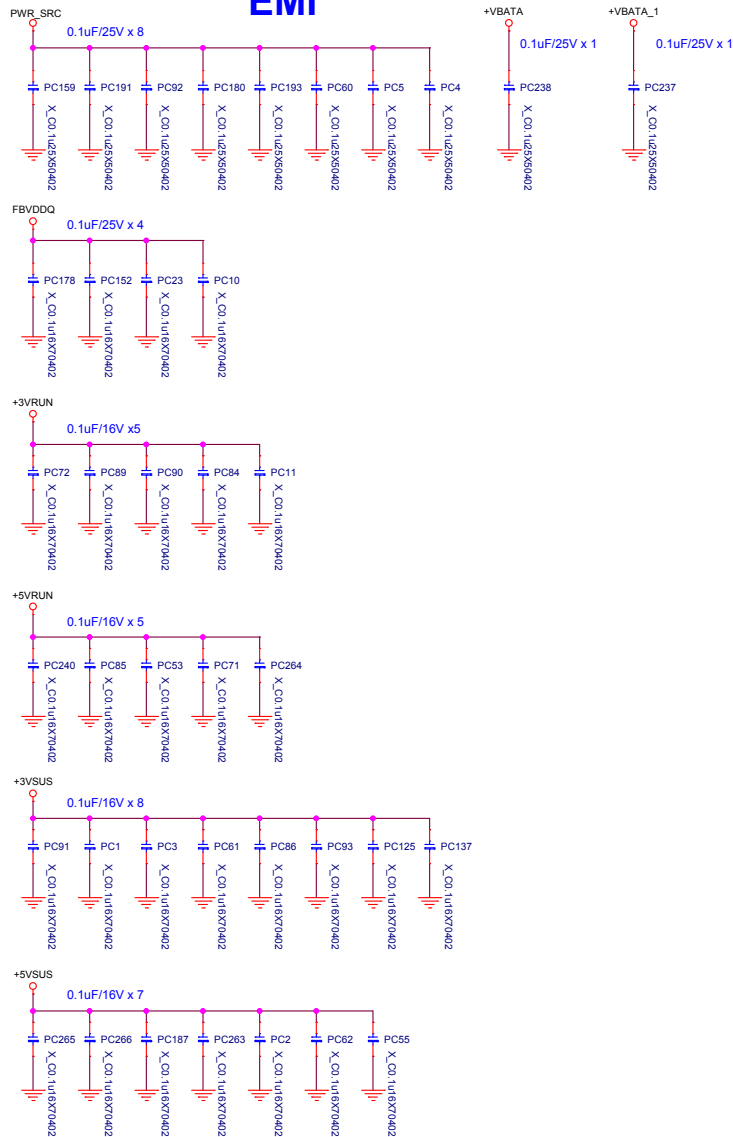
## DGPU POWER NVVDD

VBoot:0.8V

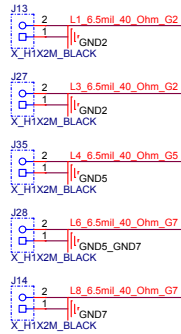
Vmin:0.5V / Vmax:1.25V



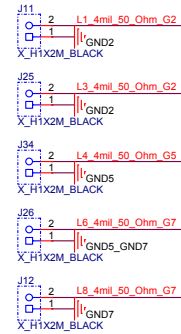
# EMI



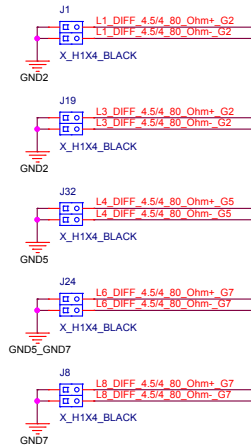
## 40 OHM Single-End



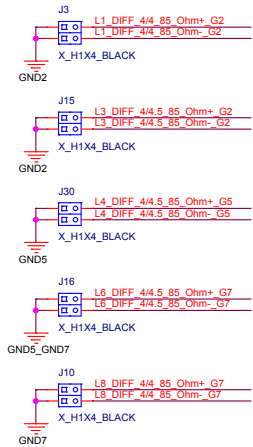
## 50 OHM Single-End



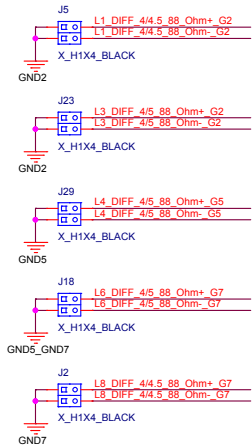
## 80 OHM Differential



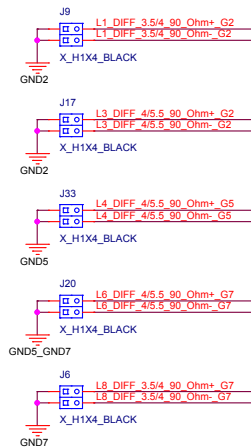
## 85 OHM Differential



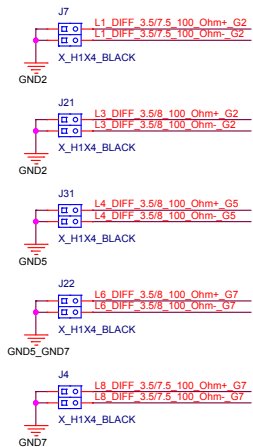
## 88 OHM Differential



## 90 OHM Differential



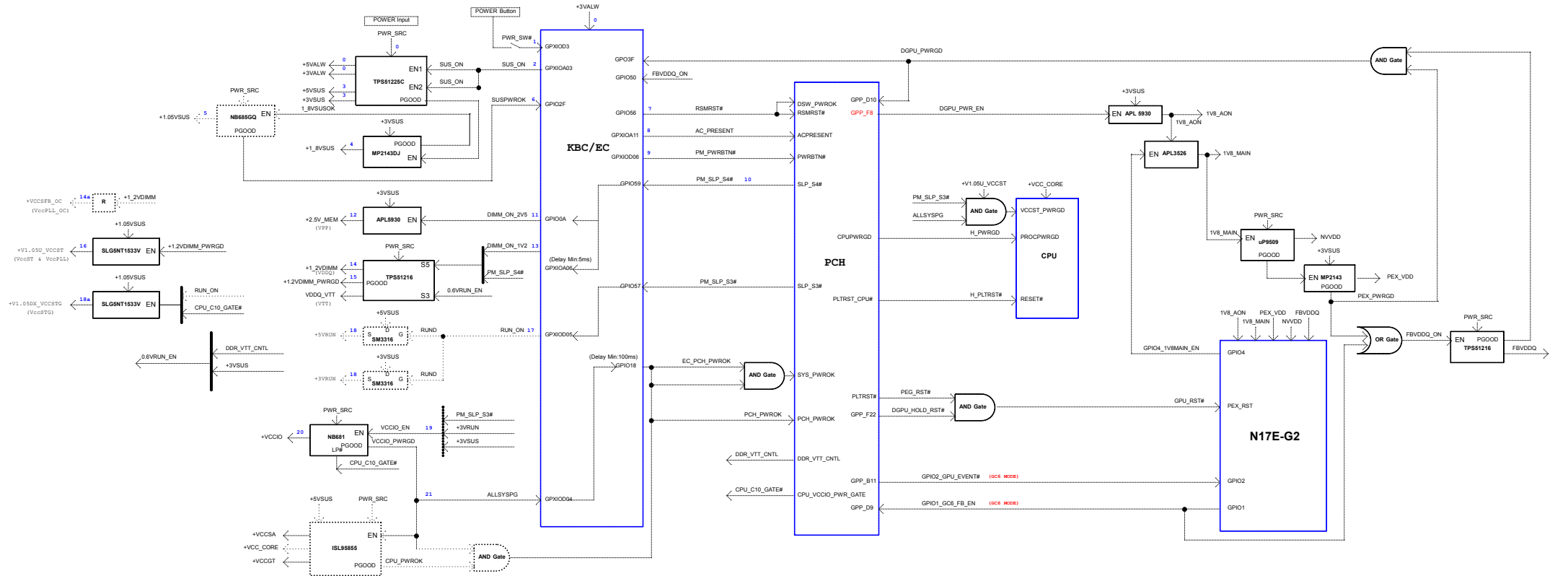
## 100 OHM Differential



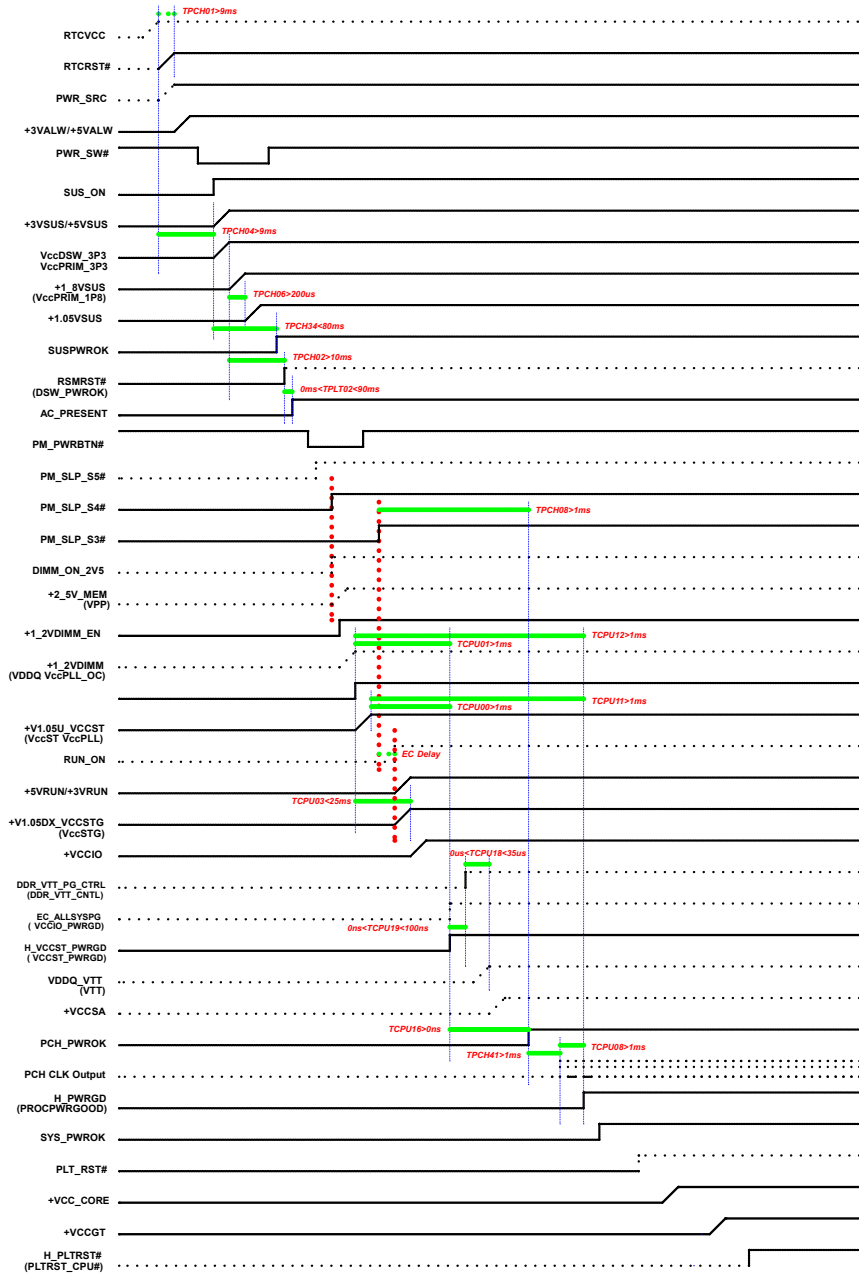




## MS-16R1 Power on Block Diagram



G3 -> S0



S0 -> G3

